Insights Into Interface Treatments in p-Channel Organic Thin-Film Transistors Based on a Novel Molecular Semiconductor

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***Abstract*— Organic thin-film transistors (OTFTs) were fabricated using a novel small molecule, C6-NTTN, as the semiconductor layer in several different architectures. The C6-NTTN layer was deposited via both vacuum evaporation at different substrate temperatures and via solution-processing, which yield maximum hole mobilities of 0.16 and 0.05 cm^2/V · s, respectively. Surface treatments of the substrate, insulator, and metal contacts used for OTFT fabrication employing polymer films and different self-assembled monolayers were investigated. In particular, in bottom-gate devices, the insulator surface hydrophobicity was optimized by the deposition of poly(methyl methacrylate) or hexamethyldisilazane, while in the top-gate geometry, pentafluorobenzenethiol was efficiently used to modify the substrate surface energy and to change the contact work function. Atomic force microscopy analysis was exploited to understand the relationship between the semiconductor thin-film morphology and the device electrical performance. The results shown here indicate an inverse proportionality between the mobility and the interface trap density, with parameters depending especially on semiconductor–insulator interfacial properties, and a correlation between the threshold voltage and the characteristics of the semiconductor–metal interface.**

***Index Terms*— Charge carrier mobility, organic thin-film transistors (OTFTs), semiconductor–insulator interfaces, semiconductor–metal interfaces, surface treatment.**

I. Introduction

ORGANIC semiconductors are of great interest thanks to the possibility of being deposited onto both rigid and flexible substrates to realize optoelectronic devices that are inexpensive, lightweight, and wearable [1], [2]. With the motivation of realizing organic devices in real applications, much effort has been done on the synthesis of novel air-stable materials [3]–[5], on the optimization of long-living devices [6] and on the investigation and modeling of the physical mechanisms underlying the device operation [7], [8].

A critical issue of particular importance in organic thin-film transistors (OTFTs) remains as the quality of the interfaces between different active layers. The localized states related to the presence of structural defects and chemical impurities concentrated there dominate the electrical performance and stability of the device. For this reason, the main concerns are typically the choice of materials and their proper layer arrangements with using right deposition processes [9]–[11]. Furthermore, proper interface treatments are introduced on substrates, insulators, or metals, often employing additional polymer thin films or self-assembled monolayers (SAMs), in order to maximize charge transport and injection efficiency [12]–[14].

Interface treatments of the OTFT material components can affect the device electrical parameters directly, as in the case of threshold voltage shifted with the use of dipolar SAMs [15], [16], or indirectly, through the change of the surface energy, roughness, and defect density, inducing modifications in the above-deposited semiconductor morphology (grain size, defect distribution) and influencing mostly the charge carrier mobility and the subthreshold swing [15], [17]. Regardless, the mechanisms behind the effects induced by the surface functionalization are still under debate.

In this contribution, we investigate the effects of various interface treatments on the performance of OTFTs based on the novel semiconductor molecule C6-NTTN, studying the relationship between electrical properties and process parameters in two device configurations [bottom-gate/top-contact (BG/TC) and top-gate/bottom-contact (TG/BC) and two deposition techniques (thermal evaporation and spin-coating]. The experimental results evidence that the carrier mobility is governed by the properties of the semiconductor–dielectric interface, especially for the evaporated films, and can be enhanced by interface treatments, whereas the threshold voltage is influenced by various factors but mainly changes with the device configuration.

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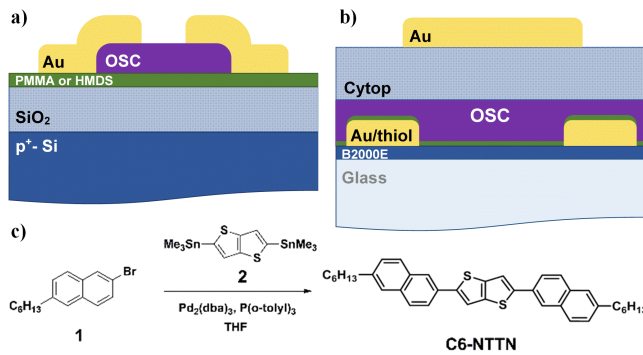

Fig. 1. Cross sections of OTFTs based on the Polyera organic semiconductor in (a) BG and (b) TG configurations; (c) synthesis and chemical structure of the novel small molecule C6-NTTN.

II. Materials and Methods

OTFTs were built in the BG/TC [Fig. 1(a)] and TG/BC [Fig. 1(b)] device configurations. The BG geometry allows accessing the gate insulator surface and performing treatments before the semiconductor deposition. The TG geometry, which is technologically preferred due to the additional role played by the dielectric layer as a barrier to environment, allows also the functionalization of the source and drain electrodes. The organic semiconductor used in this paper has a novel π-molecular structure with thienothiophene as an intermediate π-unit and alkyl-substituted naphthalene as terminal π-units. The semiconductor molecule, C6-NTTN, was synthesized via Stille cross-coupling reaction between the bisstannylated compound 1 and the corresponding monobromo-derivative 2 with $Pd_2(dba)_3/P(o\text{-tolyl})_3$ as the catalyst/ligand system [Fig. 1(c)]. The final compound is purified by flash column chromatography (85% yield). The chemical structure and purity of the final compound was confirmed by ^{1}H nuclear magnetic resonance (NMR), elemental analysis, and melting point measurement. The semiconductor molecule was found to be soluble in common organic solvents, which enables solution processing for thin-film fabrication. The details of the synthesis are reported in the Appendix. The semiconductor was processed by thermal evaporation or spin-coating techniques, both of which yield good reproducibility of the film properties. While thermal evaporation favors the growth of highly ordered films, spin coating enables inexpensive and rapid fabrication.

The BG/TC devices were fabricated starting from a p-type Si substrate, which acts as the bottom gate, and thermally grown silicon oxide (300-nm thick) used as the gate dielectric. Besides using the bare substrate, other dielectrics were prepared by covering the SiO_2 with a spin-coated thin film of poly(methyl methacrylate) (PMMA) (15-nm thick) or an SAM of hexamethyldisilazane (HMDS), in order to modulate the dielectric surface energy. Subsequently, the active layer with a thickness of about 60 nm was evaporated maintaining the substrates at either room temperature (RT) or high temperature (90 °C or 120 °C). Finally, air-stable gold electrodes (50 nm) were evaporated through a shadow mask with an aspect ratio of 10 as source and drain contacts (the width and length of the channel are 500 and 50 μm, respectively).

The TG/BC devices were fabricated on glass substrates covered by a buffer polymer layer (Polyera ActivInk B2000E), starting with the evaporated Au contacts (50 nm). Besides using bare gold contacts, a thiolated SAM, i.e., 4-aminothiophenol (ATP), pentafluorobenzenethiol (PFBT), or perfluorodecanethiol (PFDT), was spin-coated onto the substrate to study the effect of substrate surface energy modification and the metal work function. In particular, PFBT and PFDT increase the surface hydrophobicity, whereas ATP reduces it [14], [18]. On the other hand, PFDT, PFBT, and ATP change the work function of gold from 5.1 eV, respectively, to 5.44, 5.35, and 4.64 eV [14], [18]. After this stage, the semiconductor was either thermally evaporated (at RT or 90 °C) or spin-coated from a solution in dichlorobenzene (800 r/min for 90 s, postannealing at 80 °C), both of which afford a semiconductor thickness of ~50 nm. Then, a 390-nm-thick Cytop insulator layer was spin-coated at 3000 r/min for 60 s (postannealing at 100 °C) that reduces the leakage across the film to about $1.7 \cdot 10^{-10}$ A/cm^2 at 1.3 MV/cm. Finally, a gold gate electrode was evaporated.

III. Results and Discussion

The fabricated devices were electrically characterized at RT, showing typical p-channel behavior, as expected, and long-term reproducible performance both under vacuum and in ambient air. Representative output and transcharacteristics are reported in Fig. 2(a) and (b) for an OTFT without treatments. From the inset of Fig. 2(a), it is apparent that the characteristics are ohmic at low drain voltage [19]; the extracted contact resistance [20] ($R_C < 1$ MΩ) is at least one order of magnitude lower than the channel resistance in all devices, allowing a correct parameter extraction. The transfer curves in the linear region of OTFTs are shown in Fig. 2(c) and (d), respectively, for BG and TG geometries, while output and transcharacteristics of all devices at the maximum gate and drain voltage are compared, respectively, in Fig. 2(e) and (f). The curves show that the gate leakage current is higher when Cytop is used ($I_G < 10$ nA under the highest voltage) rather than SiO_2 ($I_G < 1$ nA). The fundamental electrical parameters (field effect mobility μ_{FE}, threshold voltage V_{TH}, ON–OFF current ratio I_{ON}/I_{OFF}, and subthreshold swing SS) were extracted as average value of six devices for each type and compared for the different process conditions. The equations used for the parameter extraction refer to the channel current in saturation region I_{DS}, as follows:

$$I_{DS} = \frac{W}{2L} C_i \mu_{FE} (V_{GS} - V_{TH})^2 \tag{1}$$

$$\mu_{FE} = \frac{2L}{WC_i} \left(\frac{d\sqrt{I_{DS}}}{dV_{GS}} \right)^2 \tag{2}$$

$$SS = \frac{dV_{GS}}{d(\log I_{DS})}, \quad N_{SS} = \frac{C_i}{q} \left(\frac{SS/\ln 10}{kT/q} - 1 \right) \tag{3}$$

where W and L are the width and the length of the channel, respectively, C_i is the dielectric capacitance per unit area, V_{GS} is the gate–source voltage, and N_{SS} is the maximum interface trap density (per unit area and unit energy) extracted from SS [21]. V_{TH} was evaluated as the V_{GS}-axis intersection

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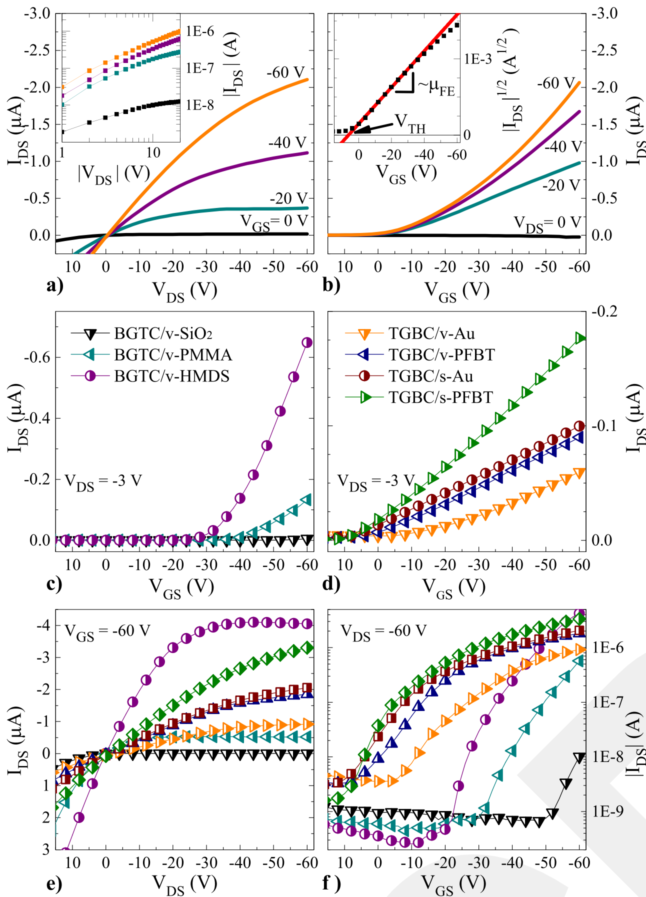

Fig. 2. (a) Representative output characteristics (inset: log-log plot at low V_{SD}) and (b) transcharacteristics (inset: V_{TH} and μ_{FE} extraction method) of a TG/BC OTFT with spin-coated semiconductor and bare Au contacts. (c) OTFT transcharacteristics in linear region for BG/TC and (d) TG/BC geometry: *v* stays for evaporated semiconductor (RT deposition) while *s* for spin-coated. (e) Output and (f) transcharacteristics of all devices.

of the tangent to $(I_{DS})^{1/2}$, as shown in the inset of Fig. 2(b), where the curve shows that the mobility is independent of gate voltage in a wide range. The insulator capacitance was measured by fabricating a metal–insulator–metal device on each substrate. The measured capacitance is 11.5, 9.5, and 11.2 nF/cm^2 for the bare, PMMA-treated, and HMDS-functionalized silicon dioxide, respectively, whereas the Cytop film has a capacitance of 4.7 nF/cm^2.

The most significant results are discussed by relating the electrical features of the devices to the semiconductor morphology observed in the channel region by the atomic force microscopy (AFM) technique, depending on the substrate temperature and surface wettability. In the TG configuration, the electrical performances are also analyzed in terms of the metal–organic–semiconductor interface.

A. OTFTs With Bottom-Gate Architecture

The charge carrier mobility measured in the BG devices with the evaporated C6-NTTN layer ranges from about 0.01 cm^2/V · s to a maximum, detected in the semiconductor deposited on a SiO_2/HMDS substrate at 90 °C, of 0.16 cm^2/V · s, while the threshold voltage ranges between

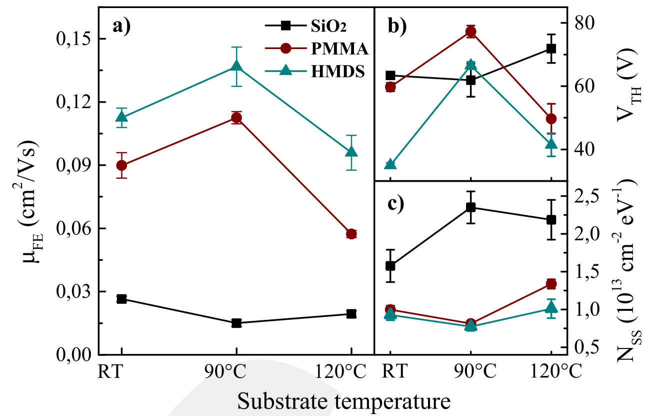

Fig. 3. Mean field-effect mobility (a) threshold voltage and (b) trap density (c) for the vapor-deposited BG/TC OTFTs as a function of the substrate temperature during semiconductor deposition, for different insulators.

−77 and −35 V. Observing the data obtained at a RT deposition, while devices on bare silicon dioxide show poor performance, the mobility and the threshold voltage result to improve for devices based on PMMA-treated SiO_2 and even more when HMDS is used, indicating that the semiconductor prefers a hydrophobic substrate. In particular, μ_{FE} increases from an average value of 0.03 cm^2/V · s on SiO_2 to 0.09 and 0.11 cm^2/V · s on PMMA and HMDS, respectively, while V_{TH} shifts from −63 V to −60 and −35 V.

Changes in the overall performances on varying the substrate temperature are not pronounced and monotonic, demonstrating that the electrical features are mainly affected by the dielectric surface. Regarding the charge carrier mobility, it is almost constant on varying the temperature for a SiO_2 substrate, whereas for PMMA and HMDS substrates, it slightly increases at 90 °C but decreases again at 120 °C [Fig. 3(a)]. In particular, the result in the case of PMMA suggests that the change of polymer surface roughness, which could occur at temperatures above its surface glass transition, does not strongly affect the nucleation and growth of the semiconductor film, differently from other organic semiconductors vapor-deposited on polymer dielectrics [22]. As for the threshold voltage, the results show that this parameter comes from the combination of multiple effects. Indeed, while for a SiO_2 substrate V_{TH} remains almost constant at all temperatures, it deteriorates at a 90 °C deposition in presence of both treatments [Fig. 3(b)]. Therefore, the improvement in relation to the insulator surface is evident especially at RT and 120 °C, but it is lost for 90 °C.

The dependence of N_{SS} on the substrate shows an improvement in presence of an interfacial treatment, with a small deterioration only at 120 °C [Fig. 3(c)]. The values range between 7 · 10^{12} and 2.3 · 10^{13} cm^{-2} eV^{-1}, comparable or slightly higher than results reported for other organic semiconductors [13]. The ON–OFF ratio is of the order of 10 for the SiO_2 substrate and between 10^3 and 10^4 for the treated substrates thanks to the higher mobility inducing elevated currents in the transistor ON-state.

The AFM analysis confirms that the semiconductor film morphology is influenced by the dielectric surface, with more

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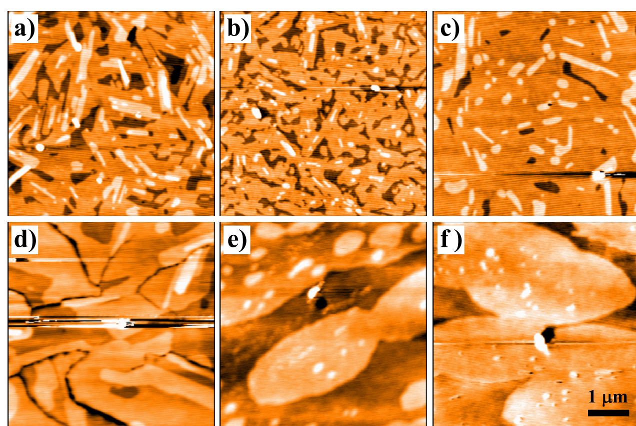

Fig. 4. AFM images of semiconductor films: (a) vapor-deposited on SiO_2 at RT, (b) on HMDS at RT, (c) 90 °C and (d) 120 °C; (e) solution-deposited on bare Au and (f) PFBT-treated contact (area around the contact).

homogeneous and interconnected grains when the film is deposited on a HMDS-treated substrate [Fig. 4(b)] than on bare SiO_2 [Fig. 4(a)]. AFM images of the semiconductor films on HMDS are also collected for the high substrate temperatures, showing that the temperature increase leads to the formation of larger grains [Fig. 4(c) and (d)], due to layer-by-layer film growth arising from enhanced molecular diffusion on the substrate surface [20]. However, with increasing temperature, the crystalline island-shaped domains growing in dimension could become less interconnected, as appear in our samples at 120 °C [Fig. 4(d)] where the polycrystalline aggregates are separated by large gaps. This phenomenon could justify the absence of an increase of the μ_{FE} for high temperatures and is consistent with the higher N_{SS} value at 120 °C.

B. OTFTs With Top-Gate Architecture

For the vapor-deposited C6-NTTN based OTFTs with a TG configuration, the influence of a PFBT treatment was studied. The SAM was found to weakly affect the charge carrier mobility but to induce a stronger variation in the threshold voltage. In particular, as regards the mobility, PFBT has a small positive effect for a RT deposition (on average 0.020 and 0.029 $cm^2/V \cdot s$ for bare and treated substrates, respectively), whereas a negative effect for a 90 °C deposition, from the highest value of 0.031 $cm^2/V \cdot s$ on gold to 0.022 $cm^2/V \cdot s$ on PFBT. Regarding the threshold voltage, although, as in the case of BG/TC devices, the deposition at 90 °C yields a deterioration of V_{TH} with bare contacts (from −11 V at RT to about −20 V), in presence of PFBT a threshold of about 0 V was measured at both deposition temperatures. This shift could be attributed to the modification of both the substrate surface energy and the metal work function. From the AFM analysis, no relevant differences appear in the semiconductor morphology, justifying the weak variation of μ_{FE} and showing that the prevalent effect of PFBT is the contact modification. Indeed, the PFBT layer increases the Au work function and, therefore, induces an electron flow from the organic material into the metal until the metal Fermi level is pinned to the positive polaronic level of the semiconductor, yielding a p-doping effect in the semiconductor at the interface [21] and a reduction of V_{TH} [22].

For the solution-deposited C6-NTTN based OTFTs, after optimizing the semiconductor deposition parameters on a bare substrate (for example, the charge carrier mobility was increased by 50% up to 0.026 $cm^2/V \cdot s$ by reducing the film deposition speed from 2000 to 800 rpm), the effect of contact functionalization was studied by using all three of the thiols. They yield different results: OTFTs fabricated with ATP and PFDT were revealed to be inactive, whereas the devices with PFBT show very good performance, with an average μ_{FE} of 0.046 $cm^2/V \cdot s$, a V_{TH} of 3 V, and an I_{ON}/I_{OFF} ratio of nearly 10^4. Quite different from evaporated devices, the threshold voltage is low for both bare and treated contacts.

The AFM analysis of the semiconductor films revealed that their surface roughness decreases with the substrate surface hydrophobicity (R_{rms} = 14.0, 3.4, and 1.1 nm with ATP, PFBT, and PFDT treatments, respectively, 7 nm on the bare substrate). The high semiconductor roughness in the case of ATP could justify the absence of conductivity, while the reduced roughness thanks to PFBT [Fig. 4(f)], compared to bare gold [Fig. 4(e)], reflects positively on the mobility. On the contrary, in PFDT based OTFTs, having the smoothest semiconductor surface, the absence of conductivity can be caused by the poor adhesion of the semiconductor film on the substrate due to the very high hydrophobicity.

C. Comparison of the Electrical Characteristics Between Different OTFT Architectures

The novel semiconductor shows acceptable performance for most of the studied conditions, indicating intrinsic good transport characteristics. Indeed, as documented in [25] and [26], the rigid core of the molecule and the external chains favor a self-assembly of the structures, enabling the π-stacking beneficial for the charge transport. Comparing the devices obtained by thermal evaporation and spin-coating deposition techniques, the former have mobilities up to five times higher than the latter.

Fig. 5 shows the correlation between the charge carrier mobility, extracted from (2), and the interface defect density, estimated from (3). Consistently with the literature on disordered semiconductors [17], [27], [28], the mobility decreases with growing N_{SS}, demonstrating that the charge transport is trap-limited. However, the behavior depends on the device configuration.

In the BG/TC geometry, the experimental data show clearly an inverse proportionality between the mobility and the interface trap density, similar to other materials [29], [30], as highlighted by the lines of slope −1 in Fig. 5 of equation $\mu_{FE} = A/N_{ss}$, where the factor A depends on each insulator. This result demonstrates, as expected, that the field effect mobility, which is affected by the imperfections in the first few monolayers of the semiconductor film at the organic-insulator interface, is directly related to the insulator surface properties. The data also show that the semiconductor–insulator interface can be improved by depositing a hydrophobic layer on the silicon oxide surface: for example, HMDS favors the reduction

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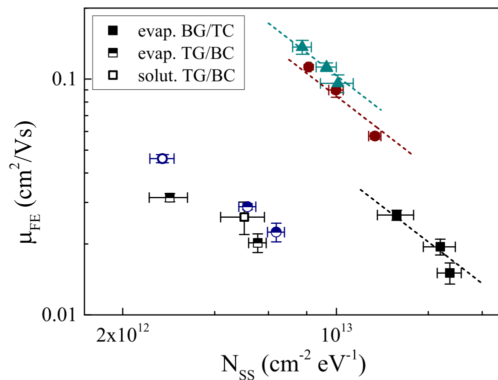

Fig. 5. Relationship between field effect mobility and trap density. Devices in BG/TC geometry with evaporated films (solid symbols) on SiO_2 (■), PMMA (•) and HMDS (▲) treatments at the three temperatures are denoted. The three lines along the data points have slope of −1. TG/BC devices with evaporated (half-solid symbol) and solution-deposited films (open symbols) on bare gold (□) and PFBT-treated contacts (○) are also marked. Multiple points with the same symbol are related to different deposition temperatures.

of the trap density in the semiconductor from $2.3 \cdot 10^{13}$ for bare SiO_2 to $7.7 \cdot 10^{12}$ cm^{-2} eV^{-1} (Figs. 3 and 5).

In the TG/BC geometry, due to the reduced number of points for each type of device, it was not possible to identify a trend of the charge carrier mobility versus the interface trap density. However, it is evident that, compared to the BG/TC geometry, the trap density is reduced, probably depending on a better interface formed between the semiconductor and the Cytop insulator [31], but the treatment carried out on the substrate has a weaker influence on the mobility. In particular, in the vapor-deposited films, the mobility remains almost constant and of the same order of magnitude as in the semiconductor vapor-deposited on SiO_2; on the contrary, the charge carrier mobility and the interface trap density are more efficaciously improved by the deposition temperature increase (as seen at 90 °C without contact functionalization). The treatment effect is more apparent in the solution deposited films where the surface roughness reduces, favoring a better semiconductor–insulator interface; however, the mobility increase is not as high as expected because of the channel length: in [32], it was demonstrated that the crystallization induced on soluble organic semiconductor by a PFBT-treated contact extends into the transistor channel for a length of about 20 μm.

Differently from the results reported in [15], [16], [28], and [33], a direct proportionality is not revealed between threshold voltage and trap density. However, a great difference in the threshold voltage arises between the BG and TG architectures, evidently because different are the regions where the treatments are carried out, and also in dependence on the semiconductor deposition technique. For BG/TC OTFTs, the treatment with a hydrophobic layer on SiO_2 seems to improve the threshold voltage, but the trend is not clear; however, V_{TH} shows generally high values in the interval from −78 to −35 V. On the contrary, in the TG/BC devices the threshold voltage assumes lower values close to 0 V. In this case, various elements are supposed to contribute to the threshold voltage improvement, with the advantage of reducing the power consumption, usually achieved by using high-k dielectrics [34]. The stability of Cytop, which is a fluorine-rich insulator and whose solvent is compatible with the underlying semiconductor, plays a fundamental role. Thanks to its high water-repellency and the absence of hydroxyl groups, this insulator forms an efficient barrier to environment and reduces the possibility of the trapping at the interface [35], as demonstrated by the reduced trap density with respect to BG devices. The optimization of the metal-organic interface has been also proven to favor the switching of the device to the ON-state [36]. Indeed, as seen for the thermally evaporated films, the threshold voltage reduces when a thiol increasing the gold work function is used. In addition to this is the substrate feature, which affects the nucleation of molecules during the semiconductor deposition and thus the film morphology. In particular, as observed in spin-coated films or in the BG devices, a hydrophobic substrate is preferable, because it yields a small semiconductor roughness, reducing the structural defects [15], with a positive effect also on the carrier mobility, although a very high hydrophobicity could be deleterious.

IV. Conclusion

Field-effect transistors fabricated with the novel organic semiconductor C6-NTTN were studied, with a particular focus on the possibility of tailoring the semiconductor/insulator and semiconductor–metal interfaces through suitable treatments, which can enhance the device electrical performance. In BG/TC devices with a vapor-deposited semiconductor film, the treatment carried out at the semiconductor–insulator interface directly affects the mobility and the threshold voltage, but the behavior depends on the substrate temperature during semiconductor deposition, which also influences the organic morphology. An evident inverse correlation was revealed between the charge carrier mobility and the interface trap density, with an improvement of the performance for a more hydrophobic insulator surface. In TG/BC devices with evaporated films, the contact functionalization affects mainly the threshold voltage, thanks to the improvement of charge injection at semiconductor–metal interface, whereas the mobility is dominated by the deposition temperature. In contrast, in the spin-coated films, the treatment influences the charge carrier mobility thanks to an enhanced crystallization of the semiconductor.

Appendix

Synthesis of 2, 5-bis(2-(6-hexylnaphthalenyl)thieno[3, 2-b] thiophene (C6-NTTN): The reagents **1** (500 mg, 1.07 mmol) and **2** (660 mg, 2.27 mmol), tris(dibenzylideneacetone) dipalladium (0) and tri(*o*-tolyl)phosphine (1:8 molar ratio $Pd_2(dba)_3/P(o\text{-tolyl})_3$; Pd loading: 0.03 equiv.) were added under inert atmosphere in anhydrous tetrahydrofuran (10 mL) and heated at 80 °C overnight. Then, the reaction mixture was cooled down to RT and precipitated into 100 ml of methanol to afford the crude product, purified by flash column chromatography on silica gel by using toluene as the eluent (0.51 g, 85% yield). m.p. 234-235 °C. ^{1}H NMR (400 MHz, CDCl3) δ: 8.06 (s, 1H),

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7.83 (d, J = 3.0 Hz, 1H), 7.81 (d, J = 3.0 Hz, 1H), 7.75 (dd, J = 8.5 Hz, 2.3 Hz, 1H), 7.62 (s, 1H), 7.60 (s, 1H), 7.38 (dd, J = 8.5 Hz, 1.6 Hz, 1H), 2.86 (t, 2H), 1.58 (m, 2H), 1.25 (m, 6H), 0.83 (t, 3H). Anal. calcd. for ($C_{38}H_{40}S_2$): C, 81.38; H, 7.19. Found: C, 81.75; H, 7.25.

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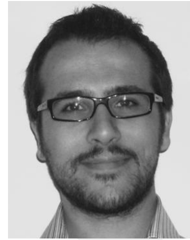

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