Interface Engineering in Organic Thin Film Transistors

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Abstract*—A novel semiconductor, the small molecule C6-NTTN, was used to fabricate organic thin film transistors (OTFTs). Different architectures and deposition techniques were employed, together with various surface treatments of the substrate, insulator and metal contacts, whose effect is analyzed through atomic force microscopy. The aim is to investigate the relationship between the process parameters and the electrical performance, with a particular attention to the quality of interfaces between active layers. The proportionality between the charge carrier mobility and the interface trap density was studied.

Keywords—organic thin-film transistors (OTFTs); semiconductor-insulator interfaces; semiconductor-metal interfaces; trap-limited charge transport.

1. Introduction

Much research effort has been done, in order to realize reliable organic devices to be employed in real applications, on the synthesis of novel semiconductors, thanks to the possibility of tailoring the material electrical and optical properties through its microstructure [1]-[4]. Clearly, the study and the modeling of the physical mechanisms underlying the device operation concur with this aim [5]-[7], allowing the device optimization. In this regard, an issue of particular relevance is the engineering of the interfaces between different layers.

The performance of organic thin film transistors (OTFTs), as well as of other devices [8]-[10], can be strongly affected by the interface properties. Therefore, tailoring the interfaces, where structural defects and chemical impurities inducing localized states are concentrated is a key strategy for the device optimization [11][12]. In this work, various self-assembled monolayers (SAM) were used in an OTFT with a novel semiconductor to study the correlation between charge carrier mobility, threshold voltage, interface trap density and material morphology.

2. Methods and Results

A. C6-NTTN Microstructure

The organic small molecule C6-NTTN has a novel π-molecular structure with thienothiophene as an intermediate π-unit and alkyl-substituted naphthalene as terminal π-units [Fig. 1(a)] [12]. The optimization of the molecular geometries and total energy calculations were performed via density functional theory prior to the synthesis. The theoretical energy levels (E_{LUMO}= 1.59 eV, E_{HOMO}= 5.09 eV) predicted a p-type behavior. The compound chemical structure and purity was confirmed by the nuclear magnetic resonance.

From the UV-vis spectrum [Fig. 1(b)] and the electrochemical measurements [Fig. 1(c)], an optical bandgap of about 2.9 eV and a HOMO level of 5.36 eV were extracted, from which a LUMO value of 2.46 eV was calculated.

The semiconductor molecule can be deposited by thermal evaporation or by solution processing, since it is soluble in common organic solvents. In this contribution, thermal evaporation and spin-coating were used, both yielding a good reproducibility of the film properties.

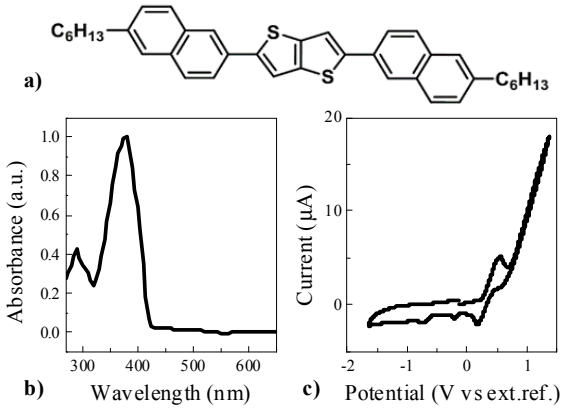

Fig. 1. a) Chemical structure of the novel molecule C6-NTTN; b) UV-vis spectrum in $CHCl_3$ solution; c) cyclic voltammetry in $CHCl_3$ solution vs. external Fc/Fc^+.

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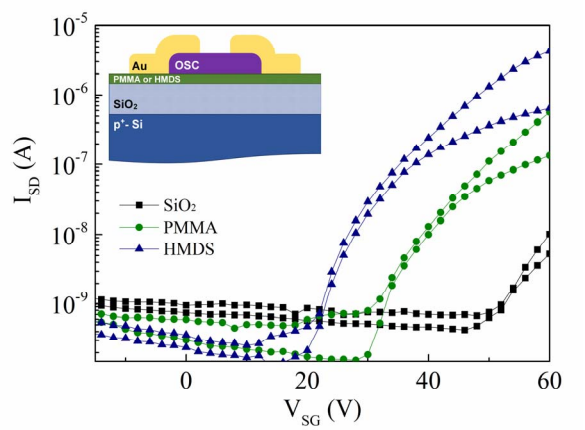

Fig. 2. Transcharacteristics in linear (V_{SD}= 3 V) and saturation (V_{SD}= 60 V) regime of BG/TC OTFTs with organic semiconductor evaporated on SiO_2, PMMA or HMDS at room temperature. Inset: cross section of BG/TC devices.

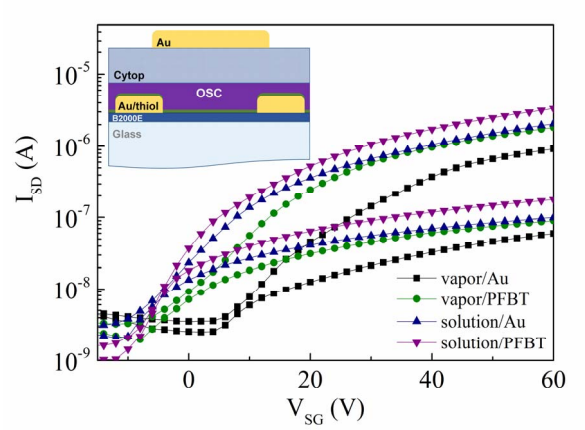

Fig. 3. Transcharacteristics in linear (V_{SD}= 3 V) and saturation (V_{SD}= 60 V) regime of TG/BC OTFTs with organic semiconductor evaporated or spin-coated on bare or PFBT-treated substrate at room temperature. Inset: cross section of TG/BC devices.

B. OTFT Fabrication

The OTFTs were realized in the bottom-gate/top-contact (BG/TC) and top-gate/bottom-contact (TG/BC) architectures. In BG/TC configuration they were fabricated on a p-type Si substrate with thermally grown 300 nm-thick silicon oxide (SiO_2), acting as the gate and dielectric, respectively. Then, the C6-NTTN with a thickness of 60 nm and gold electrodes were deposited by thermal evaporation. The TG/BC OTFTs were fabricated on glass substrate covered by a buffer polymer layer and gold contacts. Then, the C6-NTTN (50 nm) was evaporated or, dissolved in dichlorobenzene, spin-coated; a 390 nm-thick Cytop insulator layer was spin-coated and, finally, a gold gate electrode was evaporated.

The influence of the quality of the interfaces between the active layers on the device electrical performance and stability was investigated by introducing and comparing different treatments of the substrate, insulator and metal contact surfaces. With this aim, for the BG devices, three dielectrics were employed: bare SiO_2, SiO_2 covered with a spin-coated thin film (15 nm) of poly(methyl methacrylate) (PMMA) or with a SAM of hexamethyldisilazane (HMDS); while the semiconductor was evaporated with the substrate at three different temperatures: room temperature (RT), 90 °C or 120 °C. For the TG devices, other than the bare substrate, the SAM pentafluorobenzenethiol (PFBT) was used.

C. OTFT Characterization

The transcharacteristics of the fabricated OTFTs collected at RT are reported for the BG and TG configuration, respectively, in Fig. 2 and Fig. 3, at a V_{SD} of 3 V (linear regime) and 60 V (saturation regime). The contact resistance resulted to be at least one order of magnitude lower than the channel resistance and therefore allowed to correctly extract the fundamental electrical parameters, i.e. field effect mobility (μ_{FE}), threshold voltage (V_{TH}) and interface trap density (N_{SS}). The mobility and the threshold voltage were evaluated in the saturation regime from the tangent to $(I_{DS})^{1/2}$, while the interface trap density was obtained from the subthreshold swing [13]. The gate leakage current is lower than 1 nA and 10 nA for OTFTs with SiO_2 and Cytop, respectively. The insulator capacitance was extracted from a metal-insulator-metal device for each substrate and is 11.5, 9.5 and 11.2 nF/cm^2 for the bare, PMMA- and HMDS-treated SiO_2 and 4.7 nF/cm^2 for the Cytop.

The maximum μ_{FE} in the BG devices is about 0.16 cm^2/V·s, for a semiconductor vapor-deposited on a SiO_2/HMDS substrate at 90 °C, whereas in the TG devices it is 0.05 cm^2/V·s, revealed for a semiconductor spin-coated on a PFBT-treated substrate. The V_{TH} ranges between -77 and -35 V for the BG configuration and between -20 and 3 V for the TG one.

The treatment effect at the insulator surface before the semiconductor deposition in the BG OTFTs appears quite clear, with performance improved when PMMA and HMDS are used on the bare SiO_2 substrate, independently from the deposition temperature. In particular, the treatment produces the μ_{FE} increase and, in some cases, the V_{TH} reduction. Differently, in the TG OTFTs, if the semiconductor is deposited by thermal evaporation, the effect of the substrate and contact treatment is weakly visible on μ_{FE} but clearer on V_{TH} (Fig. 3), whereas, if the C6-NTTN

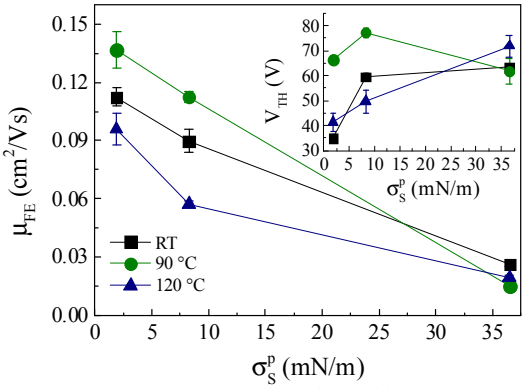

Fig. 4. Mean field-effect mobility (threshold voltage in the inset) for the vapor-deposited BG/TC OTFTs as a function of the polar component of the surface energy of the insulator, for the different substrate temperatures during the semiconductor deposition.

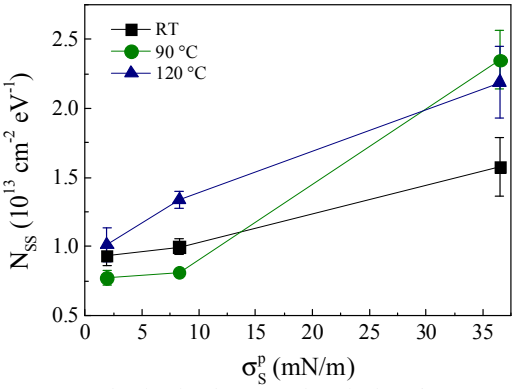

Fig. 5. Trap density for the vapor-deposited BG/TC OTFTs as a function of the polar component of the surface energy of the insulator, for the different substrate temperature during the semiconductor deposition.

is spin-coated, since V_{TH} is low also for a bare substrate, the effect is more evident on μ_{FE}.

3. Discussion

Since the device electrical parameters appear to be affected mainly by the substrate on which the semiconductor was deposited, rather than by the temperature, they were compared with the substrate surface energy, calculated through the contact angle method. Fig. 4 shows, for the BG devices, the relationship between μ_{FE} and the polar component of the insulator surface energy. Here, the SiO_2 corresponds to the least hydrophobic substrate, while HMDS surface is the most hydrophobic. V_{TH} and N_{SS} are reported in the inset of Fig. 4 and in Fig. 5, respectively. The data demonstrate that the semiconductor-insulator interface is improved by depositing on SiO_2 a hydrophobic layer. In detail, the HMDS treatment favors the increase of μ_{FE} of one order of magnitude (Fig. 4) and the reduction of N_{SS} by a factor of three (Fig. 5). Differently, V_{TH}, clearly originating from the combination of multiple effects, does not show a well-defined behavior. The AFM analysis, showing more homogeneous and interconnected grains for the semiconductor deposited on HMDS [Fig. 6(b)] than on SiO_2 [Fig. 6(a)], confirms the effect of the dielectric surface on the semiconductor film morphology and, consequently, on the charge carrier mobility.

Performance variations with the substrate temperature are not monotonic. Except for the case of SiO_2 with an almost constant mobility, for PMMA and HMDS substrates, μ_{FE} increases for a 90 °C deposition but deteriorates again at 120 °C. Differently from other organic semiconductors evaporated on polymer dielectrics [14], the growth of C6-NTTN is not strongly affected by the surface glass transition of PMMA. The AFM images collected for the semiconductor deposited on HMDS at 90 °C [Fig. 6(c)] and 120 °C [Fig. 6(d)] indicate that a higher temperature enhances the molecular diffusion on the substrate surface, favoring a layer-by-layer film growth with the formation of larger grains [14], but also show that the large crystalline aggregates formed at a very high temperature could be separated by larger gaps, becoming less interconnected and justifying the lower mobility and the higher trap density.

As regards the TG devices with spin-coated C6-NTTN, the substrate treatment with PFBT, which increases μ_{FE}, was revealed to reduce the semiconductor surface roughness from 7 nm to 3.4 nm. This was attributed to an increase of the substrate surface hydrophobicity, which, similarly to HMDS in the case of BG devices, improves the semiconductor growth. A great contribution is also given by the reduction of the potential barrier at the semiconductor-metal interface, since PFBT increases the work function of gold from 5.1 eV to 5.35 eV [11], which is aligned with the C6-NTTN HOMO level. When the semiconductor is evaporated, the AFM analysis does not show relevant differences in its morphology along the

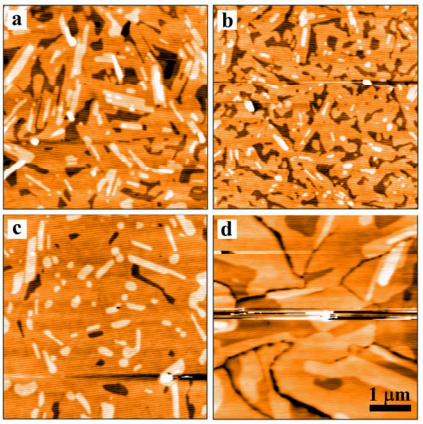

Fig. 6. AFM images of semiconductor films evaporated on SiO_2 at RT (a), on HMDS at RT (b), 90 °C (c) and 120 °C (d).

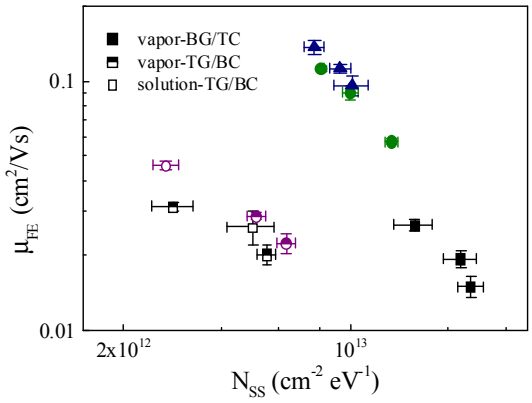

Fig. 7. Field-effect mobility as a function of interface trap density for BG/TC devices (solid symbols) on SiO_2 (square), PMMA (circle) and HMDS (triangle) at three temperatures and for TG/BC devices with semiconductor solution- (open symbols) and vapor-deposited (half-solid symbols) at two temperatures on bare (square) and PFBT-treated (circle) substrates.

channel in presence of the substrate treatment, justifying the weak μ_{FE} variation [15]. A major effect was rather revealed in V_{TH} and was attributed to the contact modification.

Comparing the two device architectures, the main difference is the threshold voltage. In the BG OTFTs it assumes high values, whereas in the TG ones it is close to zero, presumably thanks to the stability and water-repellency of the Cytop layer, which acts as an efficient barrier to the environment, as demonstrated by the reduced N_{SS}. The performance is then further enhanced by the thiolated treatment, which improves the substrate hydrophobicity and aligns the metal work function to the semiconductor HOMO level.

Finally, for all the OTFTs, the comparison between μ_{FE} and N_{SS} (Fig. 7) reveals an inverse proportionality between them [13], demonstrating that the conduction is trap-limited. Indeed, the field-effect mobility is related to the effective band mobility μ_0, through the ratio between free carrier density (n_{free}) and trapped carrier density (n_{trap}), as: $\mu_{FE} = \mu_0 \cdot n_{free}/(n_{free}+n_{trap}) \approx \mu_0 \cdot n_{free}/n_{trap}$, assuming $n_{free} \ll n_{trap}$. The product $\mu_0 \cdot n_{free}$ appears to depend on each insulator used.

4. Conclusion

OTFTs with the novel semiconductor C6-NTTN were fabricated and the role played by the insulator- and metal-semiconductor interfaces was studied. Interface trap density reduces for a lower polar component of the insulator surface energy, leading to the mobility increase. Threshold voltage improves both with the use of the Cytop insulator and by increasing the metal work function with specific treatments.

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