

Mitigation of power quality problems using distribution static synchronous compensator: a comprehensive review

ISSN 1755-4535

Received on 7th July 2014

Revised on 6th January 2015

Accepted on 23rd January 2015

doi: 10.1049/iet-pel.2014.0531

www.ietdl.org

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Abstract: Electric power quality (PQ) in distribution system has become increasingly significant subject both for end users and power suppliers with the deregulation of the electric power market. The inadequate performance of conventional compensation devices to mitigate PQ problems has revealed the use of advanced power electronics based compensation devices. Distribution static synchronous compensator (DSTATCOM) is one of the shunt connected custom power devices used to improve PQ, voltage and reactive power support and to increase the capability of the auxiliary service for utility grid. This study presents a comprehensive review of the various DSTATCOM configurations for single-phase (two-wire) and three-phase (three or four-wire) systems and control strategies for the compensation of different PQ problems in distribution systems. In addition, comprehensive explanation, comparison and discussion on DSTATCOM technology are performed. Furthermore, latest trends, practical consideration and some future research fields on DSTATCOMs are discussed in detail. This is intended to present a broad perspective on the status of DSTATCOM technology to researchers dealing with compensation of PQ problems in distribution systems.

1 Introduction

It is very important to maintain the electric power quality (PQ) within the standard limits [1–7]. Poor PQ can cause the undesirable operation of equipment, increased power losses, interference with communication lines etc. [8]. Owing to rapid developments in power electronic technology, the applications of power electronic based devices at different voltage levels in utility grid and industrial facilities are becoming increasingly widespread. The static synchronous compensator (STATCOM) is one of power electronics based devices which can be used in the framework of flexible AC transmission systems at the transmission level [5, 9] and custom power devices at the distribution level [10]. Distribution STATCOM (DSTATCOM) performs high speed control of reactive power to provide voltage stabilisation, flicker suppression, and compensates other types of PQ disturbances. In utility grid applications, DSTATCOM provides leading or lagging reactive power to maintain the system stability during transient conditions. DSTATCOM can also be applied to industrial facilities to mitigate the voltage sag/swell and flicker caused by non-linear dynamic loads [11].

DSTATCOM can be operated either as the voltage mode control or current mode control. In the voltage mode control, it can make the bus voltage to be balanced sinusoids, irrespective of the unbalance and voltage distortion in the supply side or line current. In the current mode control, it can force the source side currents to be balanced sinusoids [12].

The performance of DSTATCOM is directly related to the design of power circuit components (such as DC-bus energy storage device, output filters and type of inverter), control algorithm used to estimate the compensation signals with less calculation, switching scheme to generate the switching pulses and stability of designed control algorithm [13].

The aim of this review article is to provide a comprehensive review of previous researches on DSTATCOM. More than 150 publications are reviewed to classify them in different categories. This paper is therefore organised as follows: First, the operation principles of DSTATCOMs are presented in Section 2. Section 3 illustrates the classifications of DSTATCOMs on power circuit

structures. Section 4 describes the control methodologies and approaches including the reference signal extraction and current control methods. Section 5 presents a classification of DSTATCOMs according to compensated variables. Finally, in Section 6, latest trends and technical considerations on DSTATCOMs are discussed, which is followed by concluding remarks and future scope in Section 7.

2 Operation principles of DSTATCOM

DSTATCOM is one of the shunt connected custom power devices and consists of an inverter (voltage source inverter [VSI] is commonly preferred), DC-link energy storage device, output filter and a coupling transformer as shown in Fig. 1 [14].

VSI converts the DC voltage across the storage device into a set of three-phase AC output voltages. The generated voltages are in phase and interconnected with the utility grid through a coupling transformer. Proper adjustment of the phase and magnitude of the DSTATCOM output voltages allows effective control of active and reactive power flow between the DSTATCOM and the utility grid [15–17]. The single phase equivalent circuit of a power system with a DSTATCOM is shown in Fig. 2. V_1 , V_{Coupling} , V_{PCC} and V_S represent the inverter output voltage; the voltage drop caused by coupling impedance, the voltage at point of common coupling (PCC) and source voltage, respectively.

If V_1 is equal to V_{PCC} , the reactive power exchange between DSTATCOM and utility grid is zero and the DSTATCOM does not absorb or generate any reactive power. When V_1 is greater than V_{PCC} , DSTATCOM performs an inductive reactance connected at its terminal. The current, flows through the transformer reactance from the DSTATCOM to the utility grid, and the device generates capacitive reactive power. If V_{PCC} is greater than V_1 , DSTATCOM performs a capacitive reactance connected at its terminal. Then the current flows from the utility grid to the DSTATCOM, resulting in the device absorbing inductive reactive power [14, 18]. Fig. 3 illustrates the V-I and V-Q characteristics of DSTATCOM which explains the reactive power exchange between DSTATCOM and utility grid. In Fig. 3, V_{ref} is the nominal voltage at PCC.

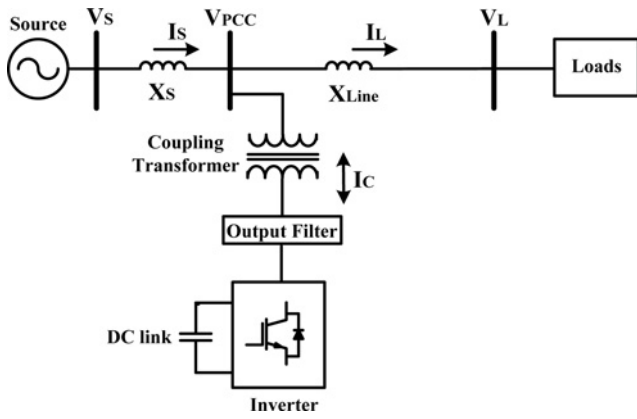


Fig. 1 Schematic diagram of DSTATCOM

DSTATCOM can manage active power flow with the utility grid by adjusting the phase angle between the DSTATCOM output and the utility grid voltages. This exchange can be used to mitigate the internal losses of the inverter and to maintain the DC capacitor charged to the proper DC voltage and thus DSTATCOM output voltage magnitude can be adjusted. Fig. 4 illustrates the vector diagram of DSTATCOM at fundamental frequency for the transition states from inductive to capacitive mode and vice versa. The transition from capacitive to inductive mode is achieved by shifting the angle δ from zero to a positive value. The active power is transferred from the DC capacitor to the utility grid and causes a voltage drop in the DC-link. The transition from inductive to capacitive mode is obtained by shifting the angle δ from zero to a negative value. The active power is transferred from the utility grid to the DC capacitor and this case causes a voltage rise in the DC-link [19].

The exchange of active and reactive power between DSTATCOM and utility grid can be calculated by (1) and (2).

$$P = \frac{V_{PCC} V_I}{X_{Coupling}} \sin \delta \quad (1)$$

$$Q = \frac{V_{PCC}^2}{X_{Coupling}} - \frac{V_{PCC} V_I}{X_{Coupling}} \cos \delta \quad (2)$$

In practical applications, power losses are not negligible. The losses on transformer windings and inverter switches are the main types of losses encountered in DSTATCOM. A small phase angle difference between V_{PCC} and V_C is added to the compensation signal to suppress these losses [20]. The power flow between the DSTATCOM and utility grid is related with DSTATCOM output voltage V_C , the utility grid voltage V_{PCC} and their phase angle differences as illustrated in Table 1 [19].

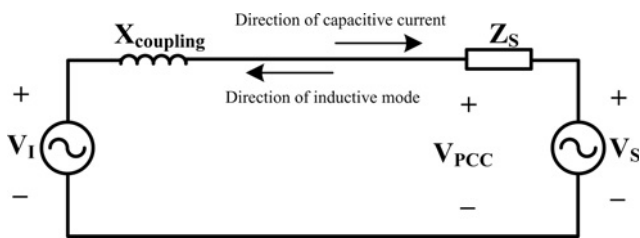


Fig. 2 Equivalent circuit of a single-phase power system with a DSTATCOM

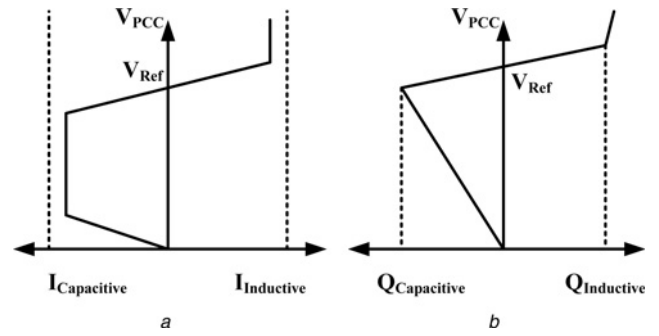


Fig. 3 The operation characteristics of DSTATCOM

- a V-I characteristics
- b V-Q characteristics

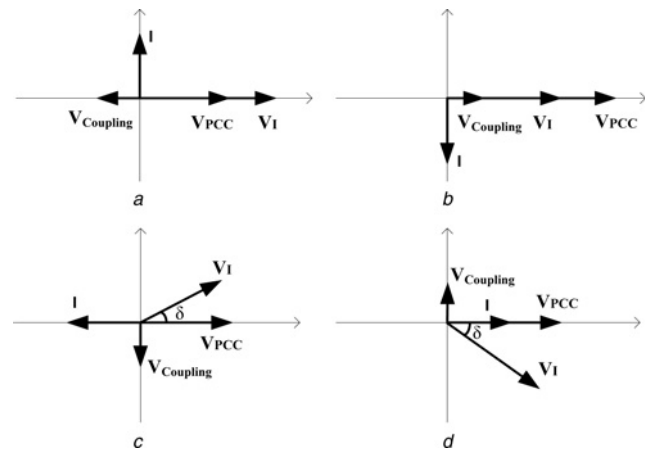


Fig. 4 Vector diagrams of DSTATCOM

- a Capacitive mode
- b Inductive mode
- c Active power release
- d Active power absorption

Table 1 Required conditions for power exchange between DSTATCOM and utility grid

Voltage relation	Power exchange		
	DSTATCOM	↔	Utility grid
$ V_I > V_{PCC} $	Q	→	Q
$ V_I < V_{PCC} $		←	
$\delta < 0$	P	→	P
$\delta > 0$		←	

3 Classifications of DSTATCOM based on power circuit structure

DSTATCOMs can be classified by their circuit structure. As shown in Fig. 5, power circuit structure of the DSTATCOM can be mainly classified into three categories namely inverter topology, type of power source and advanced configuration. Recently developed new topologies and configurations for DSTATCOM have been also discussed in this section.

3.1 Classification according to the inverter topology

As mentioned above, DSTATCOM converts the DC power across the storage device into a set of three-phase AC voltages or currents. To provide a fast and stable react in transient conditions, DC-link value must be equal to the set reference value. The inverter is responsible to regulate the DC-link voltage or current to

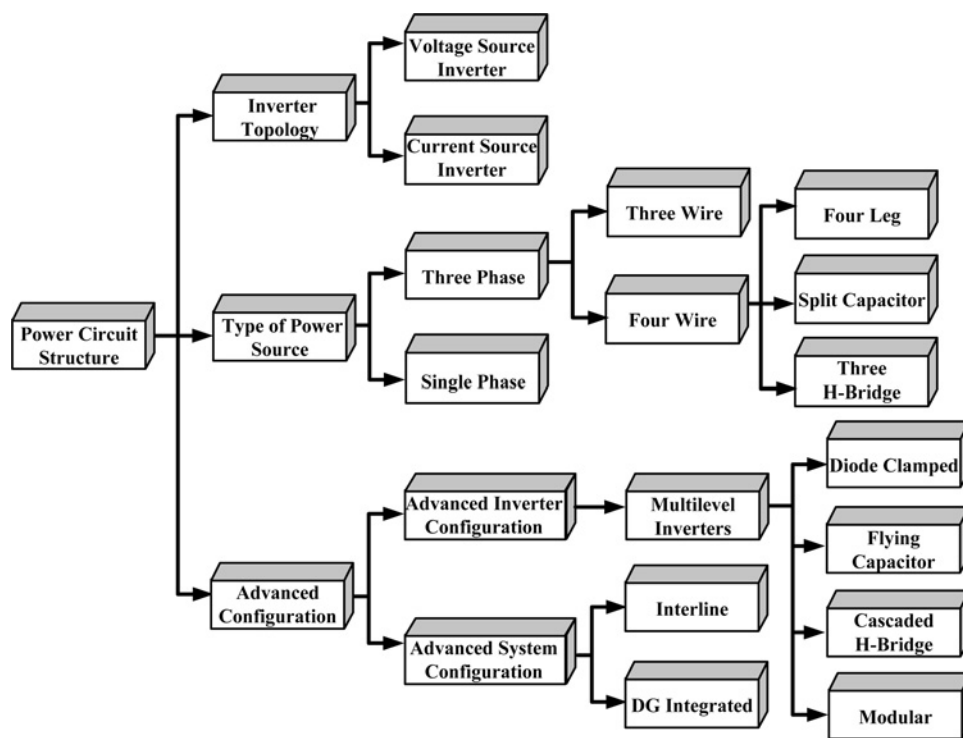


Fig. 5 Classification of DSTATCOM based on power circuit structures

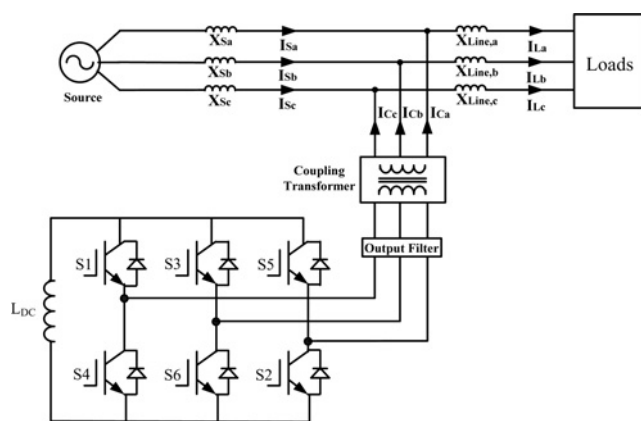


Fig. 6 CSI based DSTATCOM configuration

its reference value. DSTATCOM can be constructed with a pulse width modulated (PWM) current source inverter (CSI) [21–23] which uses a common inductor L_{DC} to form the DC bus. Fig. 6 shows the configuration of CSI-based DSTATCOM system which has the advantages of its inherent boost characteristics, longer lifetime of the storage device, fault protection capability and direct control of the output current [24, 25]. Higher conduction losses of employed inductors as energy storage devices in CSI-based DSTATCOM is the main reason of the CSI topology not becoming as popular configuration [26, 27]. However, with the development of superconducting magnetic energy storage technologies, the problem related to conventional inductors are going to be solved and hence CSIs can be considered appropriate for high power application. Moreover, the recently introduced reverse blocking IGBT has eliminated the need for series diode and thus making CSI a good alternative [28, 29].

The second topology, a most popular and common inverter topology for DSTATCOM, is PWM VSI that uses a common capacitor C_{DC} . Fig. 1 shows single-line configuration of a VSI

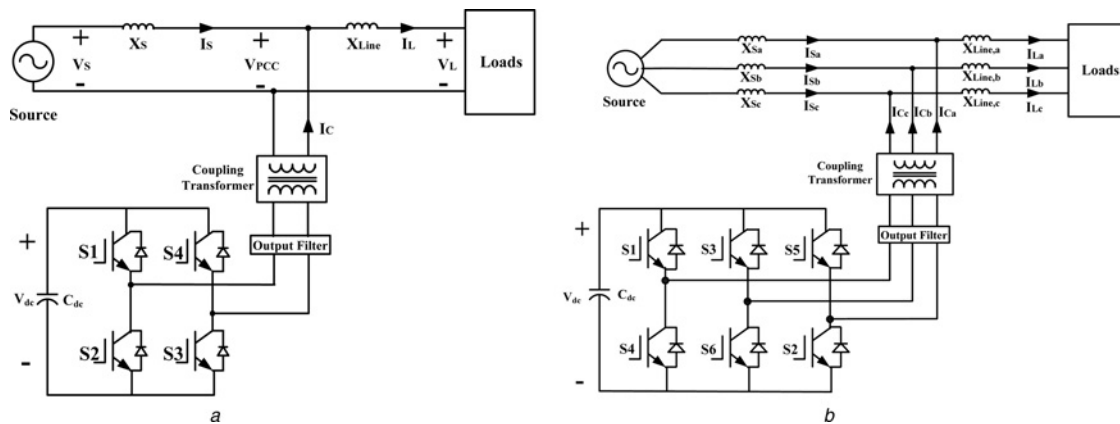


Fig. 7 The commonly used DSTATCOM configurations

- a 1P2 W VSI based DSTATCOM
- b 3P3 W VSI based DSTATCOM

based DSTATCOM. VSI topology is no need of blocking diodes, lighter in weight, flexible control and cheaper than CSI topology.

3.2 Classification according to type of power source

Generally, AC loads on the power system can be classified into single-phase and three-phase, according to supplied by single-phase (2-wire) or three-phase (3-wire or 4-wire) source, respectively. To mitigate PQ disturbances from the system, various DSTATCOM configurations are introduced and they can be classified based on the type of the supply system configurations. The voltage related PQ disturbances have similar characteristics for both single-phase and three-phase systems. In addition, three-phase systems need voltage unbalance compensation capability to provide enhanced PQ. In single-phase systems, reactive power and current harmonics are the main drawback. In three-phase three-wire (3P3 W) system, one must consider the current unbalance expected from the reactive current and current harmonics. In addition in three-phase four-wire (3P4 W) system, an extra neutral current compensation loop should be applied to eliminate the neutral current [8].

Fig. 7a shows the most common DSTATCOM configuration consisting of two H-bridge inverters in single-phase 2-wire (1P2 W) system to mitigate the PQ disturbances [30–33]. Apart from non-linear loads fed from 3P3 W system, such as adjustable speed drives, AC–AC converters, arc welding devices, and arc furnaces, cause several PQ problems. A most preferred 3P3 W VSI-based DSTATCOM configuration is shown in Fig. 7b. Furthermore, the loads in industrial facilities are often the combination of single-phase and three-phase loads supplied by 3P4 W source.

In 3P4 W distribution system, the neutral line current has major role in unbalanced supply system. Generally, its value can take up to 1.73 times of phase current [34]. Thus, fourth wire can cause an additional neutral line current flow and need extra compensation requirement. To eliminate the neutral line current in 3P4 W system, different DSTATCOM configurations have been applied, mainly, two split capacitor (2C) [35–39], four-leg (4 L) [39–44] and three H-bridge (3HB) [12, 45–52]. In 2C topology, DC-link consists of two capacitors which are connected in split as shown in Fig. 8. The midpoint of the capacitors provides a connection point for the fourth wire. In this topology, to prevent the flow of circulating current in the fourth wire, the voltages on the capacitors must be kept equal. For this aim, additional control loop is required to balance the capacitor voltages.

An additional leg (two switching devices) is used in 4 L topology to eliminate the neutral line current as shown in Fig. 9. 4 L topology can satisfy superior control over neutral line current with the use of

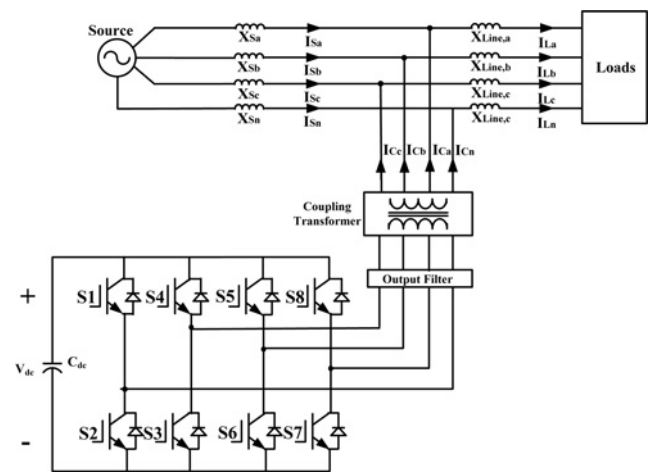


Fig. 9 4 L inverter based 3P4 W DSTATCOM configuration

fourth leg. 3HB topology is composed of three single-phase H-bridge inverters tied to the common DC-link as shown in Fig. 10.

Furthermore, in DSTATCOM systems, different connection types of coupling transformer can be applied for the neutral line current compensation. Some of the used connection types are star-delta [14, 53–56], zigzag [57–59], T connection [60–62] etc.

3.3 Classification according to the advanced configurations

This section presents a detailed review on the advanced inverter topologies and system configurations used in DSTATCOM.

3.3.1 Advanced inverter topologies: Different inverter configurations and topologies are applied to compensate PQ disturbances and to ensure the standard limits. DSTATCOM performance is directly related to the design of power circuit components. In medium voltage and high power applications, multilevel inverter technology is a very efficient alternative for DSTATCOM. The superior harmonic spectrum, decreased voltage rating for the switches, decreased common mode voltages and lesser voltage changes (dv/dt) are important advantages of multilevel inverters. However, the complexity of control method rises compared with the traditional two-level inverter. In this section, the classification of voltage source multilevel DSTATCOM is given.

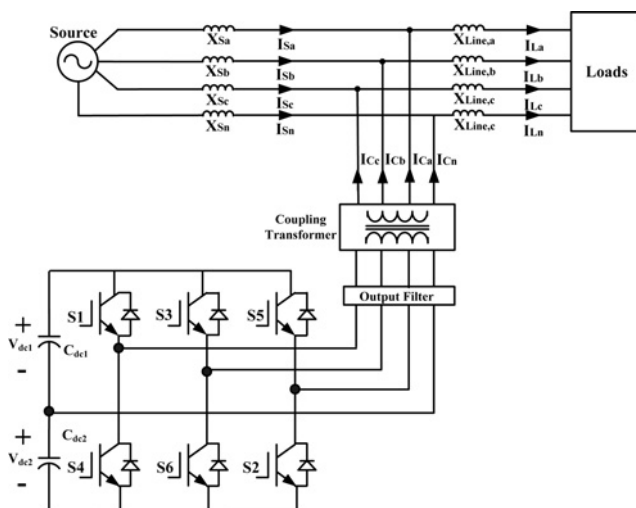


Fig. 8 2C inverter based 3P4 W DSTATCOM configuration

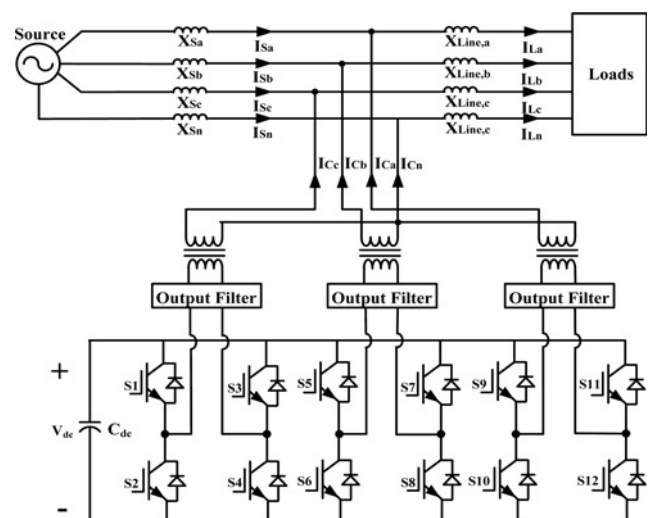


Fig. 10 3P4 W DSTATCOM based on 3HB inverter topology

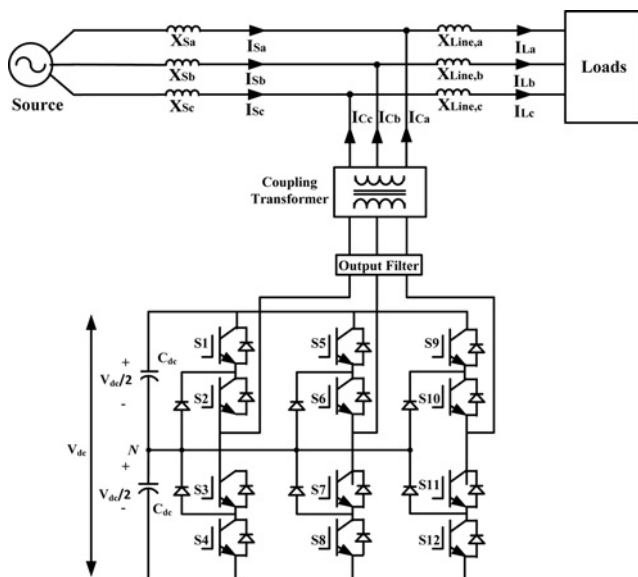


Fig. 11 Configuration of a three-level NC-DSTATCOM

Neutral point clamped DSTATCOM (NPC-DSTATCOM): NPC-DSTATCOM is comprised of double two-level VSIs stacked one over the other [38, 63–65]. As shown in Fig. 11, the negative point of the upper inverter and the positive point of the lower one are assembled together to constitute the new phase output, while to make the neutral point N , the initial phase outputs are connected via two clamping diodes. Each power switch has to block solely half of the entire inverter voltage; hence the power rating of the inverter can be doubled. NPC-DSTATCOM topology can be expanded to more output voltage levels and higher power rates by adding further power switches and clamping diodes to be able to block higher voltages [66].

Here the name diode clamped (DC) makes more sense, since there are more voltage-level clamping nodes than only the neutral N [36, 67, 68]. The clamping diodes need completely various voltage ratings for reverse voltage blocking because each triggered switch is required to block a voltage level of $V_{dc}/(m-1)$. The number of diodes needed for each phase can be determined by $(n-1) \times (n-2)$, where n represents the levels of inverter. In DC-DSTATCOM, if n represent the numbers of levels, the number of DC side capacitors can be calculated by $(n-1)$. Moreover, the freewheeling diodes number in per phase, and the clamping diodes number can be determined by $2(n-1)$ and $(n-1) \times (n-2)$. Fig. 12 shows the configuration of a three-level DC-DSTATCOM.

DC-DSTATCOMs are efficient in applications operating at fundamental frequency switching. However, the number of

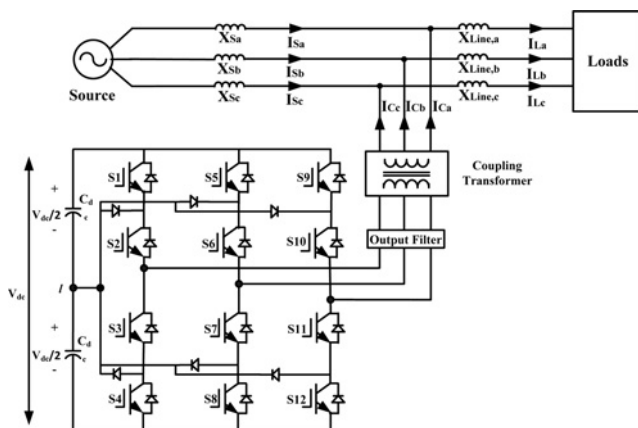


Fig. 12 Configuration of a three-level DC-DSTATCOM

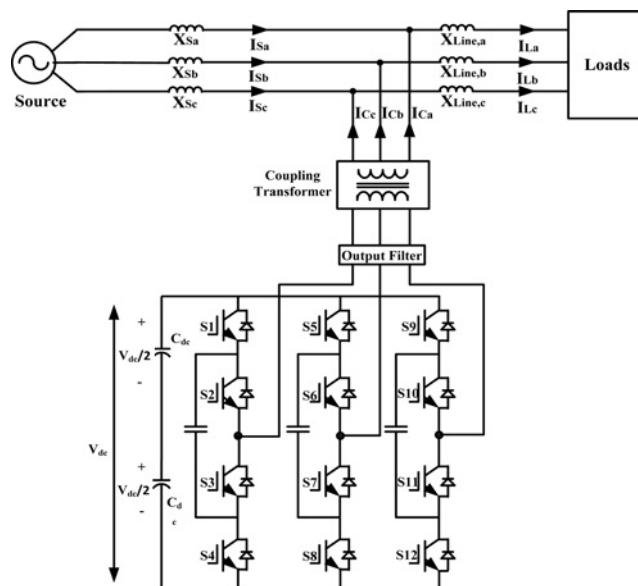


Fig. 13 Configuration of a three-level FC-DSTATCOM system

clamping diodes needed is quadratically associated with the number of output voltage levels [69].

Flying capacitor DSTATCOM (FC-DSTATCOM): FC-DSTATCOM topology is similar to the NPC-DSTATCOM expect that the clamping diodes are replaced by flying capacitors [68, 70, 71]. Fig. 13 shows a three-phase three-level FC-DSTATCOM topology where the load cannot be directly connected to the neutral of the inverter to generate the zero voltage level. Instead, the zero level is achieved by connecting the load to the positive or negative side through the flying capacitor with opposite polarity respect to the DC-link [66]. In n -level structure, NPC-DSTATCOMs require $(n-1)$ DC-link capacitors and $(n-1) \times (n-2)/2$ auxiliary capacitors per phase compared with DC-DSTATCOM topology. The most important difference between the NPC-DSTATCOM and FC-DSTATCOM topologies is that FC-DSTATCOM has a modular structure and can be more easily extended to perform more voltage levels and higher power ratings [69].

Cascade H-bridge DSTATCOM (CHB-DSTATCOM): CHB-DSTATCOMs are composed of the series connection of two or more single phase H-bridge inverters as shown in Fig. 14 [15,

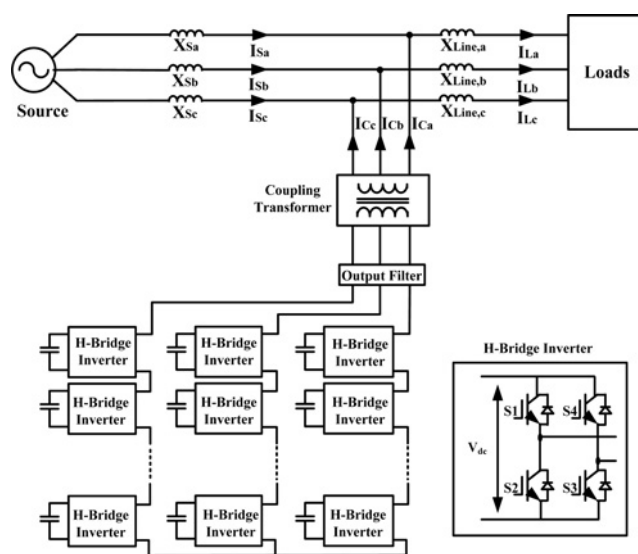


Fig. 14 Configuration of CH-DSTATCOM system

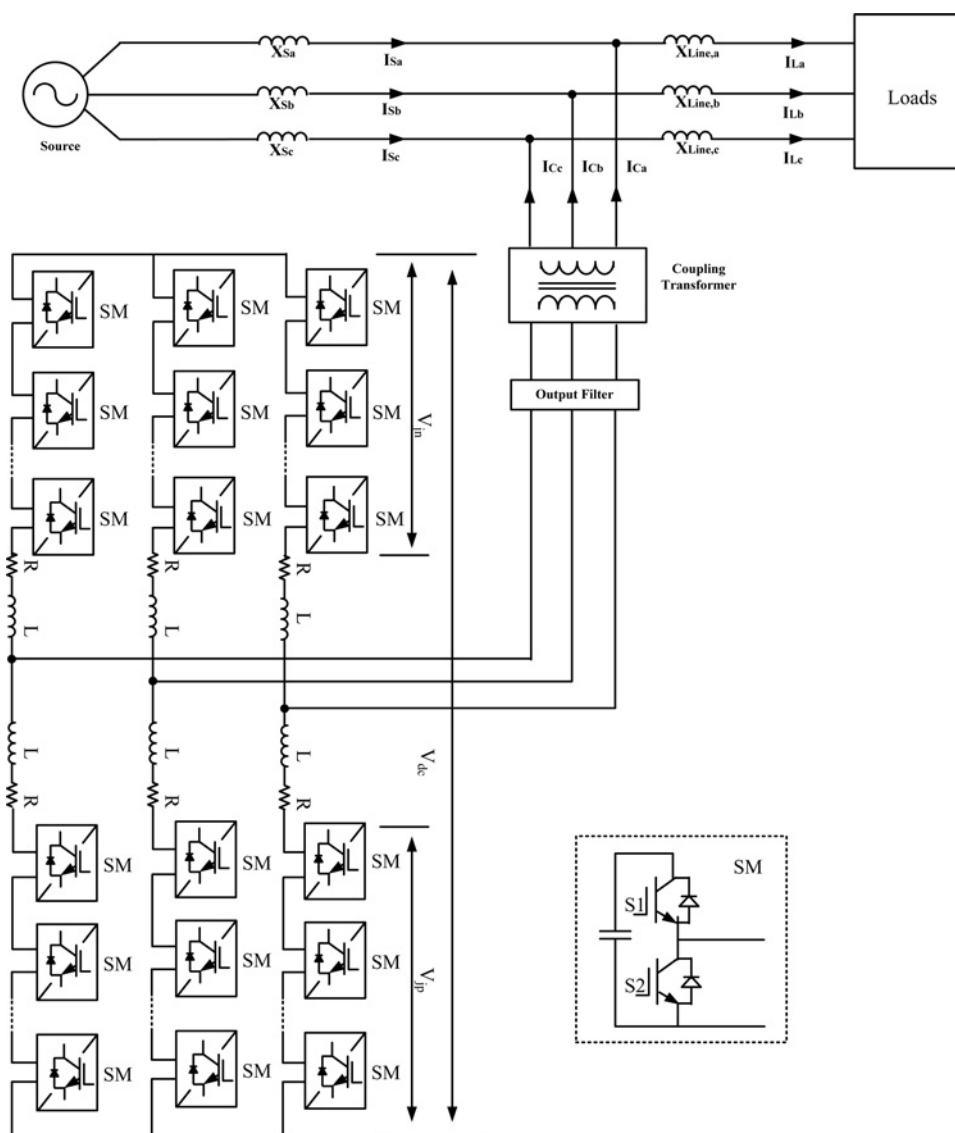


Fig. 15 Configuration of *M-DSTATCOM*

54, 59, 72–76]. In the two series connection of single phase H-bridge, each H-bridge inverter corresponds to two voltage source phase legs, where the line to line voltage is the inverter output voltage. Therefore a single H-bridge inverter can generate three different voltage levels. To avoid DC-link capacitor being short circuit, each leg has two possible switching positions. The zero level can be obtained connecting the phase outputs to the positive or the negative sides of the inverter.

The number of output phase voltage levels in a CHB-DSTATCOM with ‘*s*’ separate DC sources is ‘ $n = 2s + 1$ ’. The duty cycle for each voltage level can be adjusted so that each DC source and bridge shares the same load [6]. If *m* is assumed as the series connected modules number, the number of output voltage levels in each phase can be calculated as $2m + 1$. The switching states of *n* levels can be calculated as 3^n . The series connection of H-bridge inverters with one redundant switching state for each H-bridge inverters inherently introduces more redundancies. CHB-DSTATCOM provides more redundancies than NPC-DSTATCOM and FC-DSTATCOM topologies. These switching redundancies and the natural modularity of CHB-DSTATCOM enable the fault tolerant operation [66, 69, 77].

Modular DSTATCOM (M-DSTATCOM): The modular multilevel inverter-based DSTATCOM (M-DSTATCOM) is composed of two parallel connected complementary half-bridge cascaded converters (HBCC) as shown in Fig. 15. Each star-connected

HBCC is connected to the network by an inductive filter, while one HBCC has a negative point (NCP), the other one has a positive common point. The number of levels, in a general, $(n + 1)$ -level MMC is defined by the available *n* identical half-bridge module cascaded in each leg. All sub-modules (SM) have the same semiconductor ratings as well as dc-link capacitance, while voltage regulation of each capacitor is achieved without any additional connections or energy transformation [78].

A novel strategy to assemble an inverter with a high number of pulses by combining one twelve-pulses inverter with a seven-level inverter to attain the overall 84-pulses VSI performance with the associated clean voltage wave in [79]. As shown in Fig. 16, the associated seven-level stage is built with the combination of two three-level asymmetric inverters. By applying this novel structure, total harmonic distortion (THD) level of VSI output is reduced. The proposition allows savings in the total amount of employed switches along with having a small quantity of capacitors to prevent unbalance problems.

A five-level inverter based DSTATCOM with reduced number of switches is presented in [80] as illustrated in Fig. 17. The level shifted carrier based sinusoidal pulse width modulation (SPWM) method is used for switching. The four semiconductors in introduced inverter are switched at the SPWM frequency and two semiconductors are controlled at fundamental frequency. Such an inverter operation is suitable if the flying voltage sources which

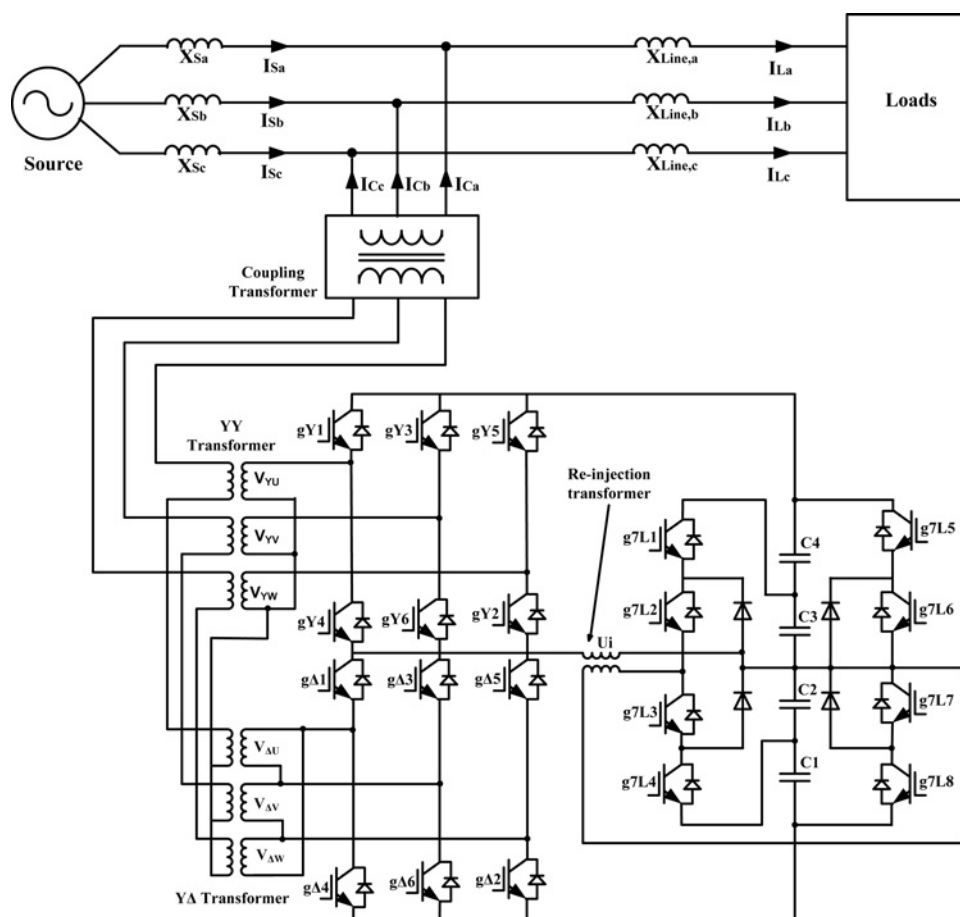


Fig. 16 Configuration of 84 pulse DSTATCOM configuration

are the capacitors do not supply average power and has zero average current over the period. The reduced number of solid state devices and their drive circuits provides an advantage over conventional H-bridge inverter.

3.3.2 Advanced connection configurations: DSTATCOM is generally connected in parallel with utility grid. Apart from this,

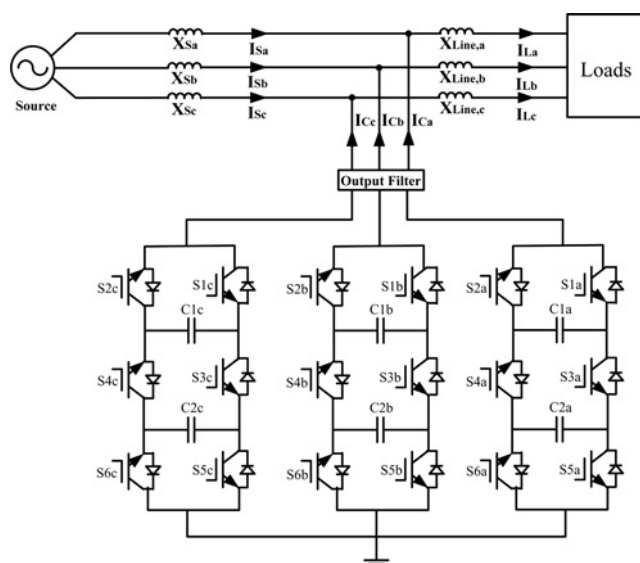


Fig. 17 Configuration of five-level DSTATCOM configuration in [80]

DSTATCOM can be utilised in different configurations. This section describes the advanced configurations of DSTATCOM.

Interline DSTATCOM (I-DSTATCOM): It is possible to use a common DC-link for several DSTATCOMs if the DSTATCOMs are installed in two or more adjacent feeders. This structure named as I-DSTATCOM enables active power exchange between two or more DSTATCOMs and thus extends the compensating range of separate DSTATCOMs as shown in Fig. 18. In an I-DSTATCOM configuration, the required active power for any DSTATCOM in the faulty feeder(s) can be supplied from other feeders through a common DC-link. Therefore it would seem at first glance that the DSTATCOMs in an I-DSTATCOM configuration can be designed to operate in phase-mode, since active power is always available [81].

Distributed generators integrated with DSTATCOM (DG-DSTATCOM): DSTATCOM can be utilised as interfacing device between distributed generation (DG) resources and utility grid and named DG-DSTATCOM as illustrated in Fig. 19 [53, 82–87]. The generated power from DG resources can be regulated and controlled through DSTATCOM which increases auxiliary service of the system and mitigates the current and voltage quality problem. DG-DSTATCOM system can provide additional advantage by delivering the uninterruptible power to the load during voltage interruption. In addition, DG resources can be operated in interconnected mode or islanding mode.

The coupling transformer links the DSTATCOM to the utility grid to satisfy proper isolation. However, many of the presented topologies for DSTATCOM can be directly connected into utility grid without coupling transformer. Among these topologies, multilevel inverter based topologies are widely preferred in high-power applications because of their capability to provide high output voltage, lower switching power dissipation, lower harmonic distortion and lower electromagnetic interference outputs [88]. DC-DSTATCOM [89], CML-DSTATCOM [90, 91] and M-DSTATCOM [92] are widely used multilevel inverter topologies.

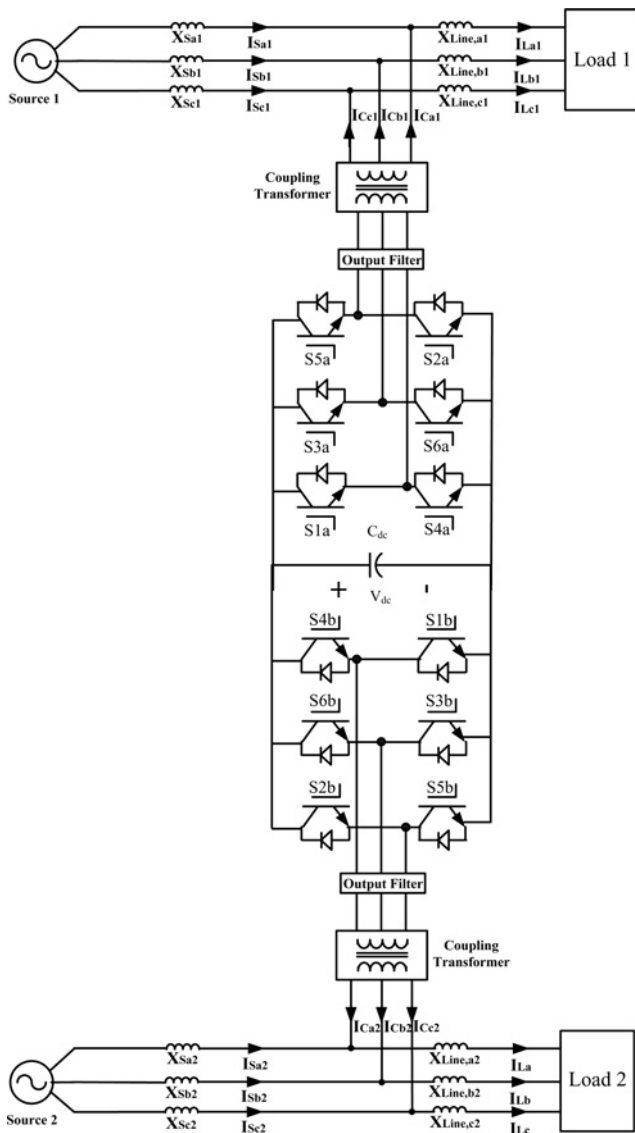


Fig. 18 I-DSTATCOM configuration

4 Classification of DSTATCOMs based on control techniques

Control strategy is the heart of the DSTATCOM and is realised in three steps. In the first step, the voltage and current signals are sensed to obtain accurate system parameters. In the second step, current or voltage compensation signals are generated based on control algorithms and DSTATCOM configurations. In the third

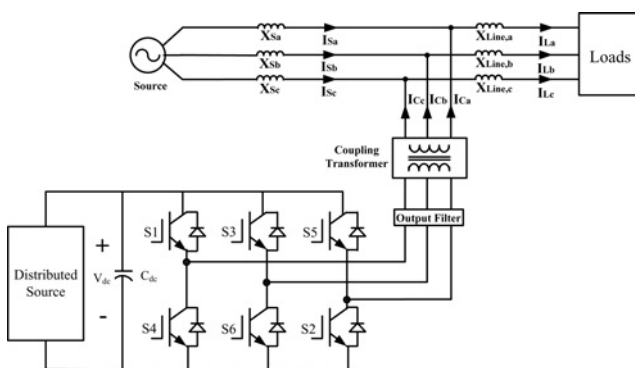


Fig. 19 DG-DSTATCOM system configuration

step, the gating signals for the power switches are produced using PWM, hysteresis, sliding-mode, or ADELIN based control techniques. The control of the DSTATCOM is performed using digital devices or advanced microelectronic devices, such as single-chip microcomputers, DSP's, FPGA's etc. [93].

4.1 Reference signal extraction techniques

The development of real-time methods for the detection and analysis of disturbances is a major concern to evaluate the quality of supply voltage and to prevent the harmful effects on equipment. The performance of a DSTATCOM strictly depends on its reference signal generation technique. In general, frequency-domain and time-domain methods are used to generate the reference signal. The time-domain methods are faster and easy to implement than the frequency-domain methods but they present worse detection performance than the frequency-domain methods. Fig. 20 illustrates the classification according to reference signal extraction techniques used in DSTATCOM.

(1) *Frequency-domain methods*: Frequency-domain methods are suitable for both single and three-phase systems. They are mainly derived from the Fourier analysis and include the following three subdivisions.

(i) *Fast Fourier transform (FFT)*: A FFT is used to compute the discrete Fourier transform (DFT) and inverse of it. A Fourier transform converts functions from time to frequency domains and vice versa. FFT computes such transformations by factorising the DFT matrix into a product of sparse factors. In DSTATCOMs, FFT is used to extract the harmonic components from the harmonic polluted signals. Owing to excessive computation in on-line application of FFT, it has high response time [93, 94].

(ii) *Kalman filter*: Kalman filter is a recursive optimal estimator and requires a state variable model for the parameters to be estimated and a measurement equation that relates the discrete measurement to the state variables. Kalman filter uses a mathematical model of the states to be estimated and suitable for real time applications. If the harmonic contents have a time varying amplitude, Kalman filter-based algorithm tracks the time variation after the initialisation period [34, 51, 94, 95].

(iii) *Wavelet transform base algorithm*: This method is based on the definition of the active and reactive power in the time-frequency domain using the complex wavelet transform. The voltage and current signals are transformed to the time-frequency domain using the complex wavelet with scaling and translation parameters to set the frequency range and localise the frequency, respectively [42, 84, 94].

(2) *Time-domain methods*: The following time-domain approaches are mainly used for three-phase systems.

(i) *p-q Theory*: In p-q theory, voltages/currents of 3P3 W system are converted into two-phase voltage/current components by Clarke transformation on orthogonal $\alpha-\beta$ coordinates, thus the instantaneous active and reactive powers can be determined without any time delay. P-q theory provides a theoretical validation that the instantaneous active and reactive powers are uniquely related with the instantaneous active and reactive currents, respectively, in 3P3 W systems. P-q theory does not follow power conservation and conflicts with the general understanding of power in that the zero sequence instantaneous reactive power cannot be defined by this theory in 3P4 W systems [43, 46, 47, 49, 96-104].

(ii) *Synchronous detection theory*: This technique, is similar to p-q theory, and comprises of three approaches-equal power, equal current and equal resistance criterion. The average power is calculated and divided equally between the three phases. In synchronisation process, the compensation signals are synchronised with relative utility grid phase voltage. It is easy theory to implement but it is affected from voltage harmonics [105, 106].

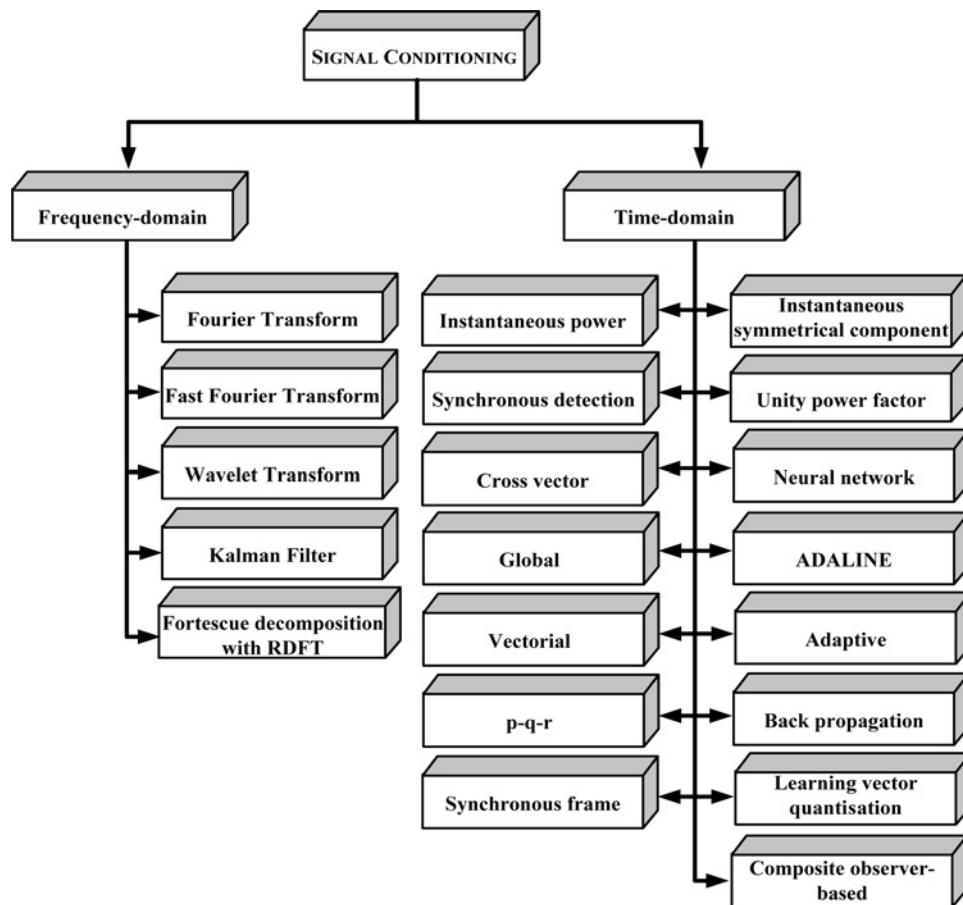


Fig. 20 Classification according to reference signal extraction techniques

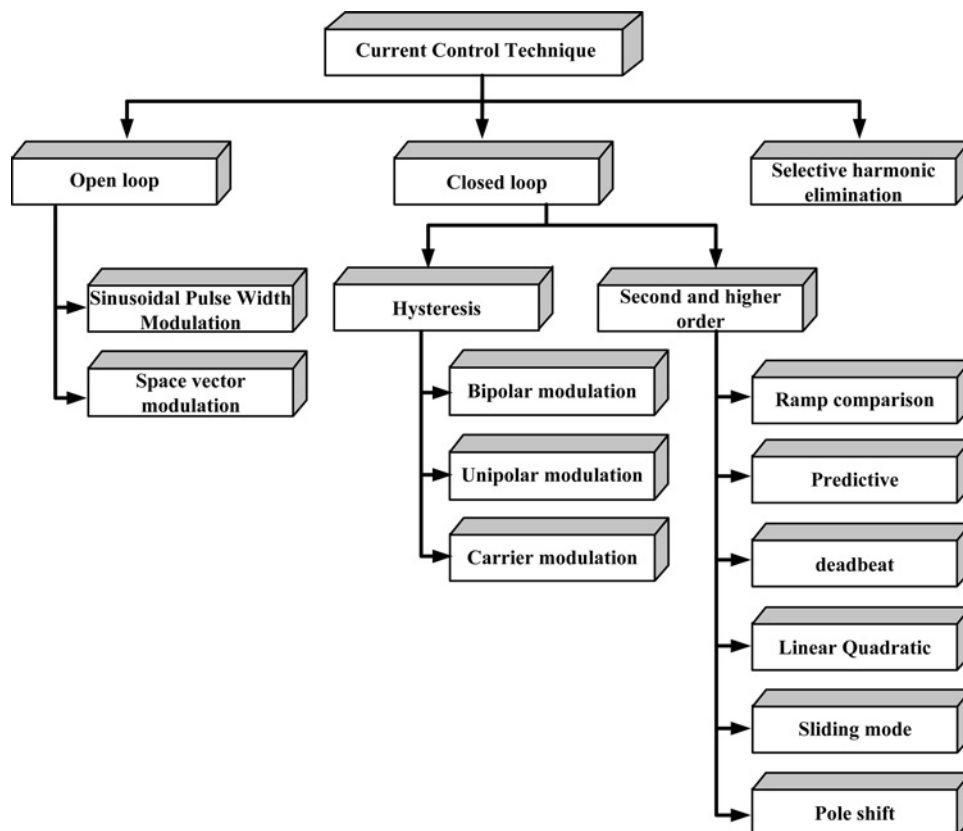


Fig. 21 Classification of current control methods

(iii) *Cross vector theory*: In cross vector theory, the instantaneous active and reactive power is defined by scalar/vector product of the voltage and the current space vectors in a 3P4W system. Cross vector theory identifies one instantaneous active power and three instantaneous reactive powers. However the three components of instantaneous reactive powers are linearly dependent to each other. In the presence of a zero sequence voltage, the neutral line current cannot be eliminated completely by compensating the instantaneous reactive power [98, 104, 107, 108].

(iv) *Global theory*: Since the reference compensation currents are determined in the A-B-C reference frame, there is no reference-frame transformation requirement. Therefore the global theory gives less complexity in realising the control circuit of the DSTATCOM. By using this theory, DSTATCOM able to compensate reactive power and suppress harmonic/neutral currents of the imbalanced/distorted load without supplying or consuming real power [98, 109].

(v) *Vectorial theory*: In this method, vectorial formulation does not need to undergo any kind of coordinates translation. Vectorial theory utilises the same power variables as p - q theory and identifies the instantaneous reactive power in phase coordinates. The current vector is split into three components. The first one is collinear with respect to the modified voltage vector, and it transports the instantaneous real power. The second one is collinear with respect to the zero-sequence voltage vector, and it transports the instantaneous zero-sequence power. The last one is normal with respect to the modified and zero-sequence voltage vectors, and it transports the instantaneous imaginary power [98, 110, 111].

(vi) *p - q - r theory*: The p - q - r theory takes the advantages of both p - q theory and cross vector theory. The defined instantaneous powers follow power conservation. Both instantaneous active and reactive powers can be defined in the zero sequence circuit in three-phase four-wire systems. The three power components are linearly independent of each other. In the presence of a zero sequence voltage, the neutral line current can be eliminated completely by applying the p - q - r theory [98, 104].

(vii) *Synchronous frame-based theory*: This algorithm is based on the transformation of the three-phase system into synchronously rotating frame to extract the direct, quadrature and zero-sequence components of signals. The active and reactive components of the system are defined by the direct and quadrature components, respectively. The high-order harmonics still remain in the signal; however they are modulated at different frequencies. These are the undesired components to be eliminated from the system and they represent the reference harmonic current. The system is very stable since the controller deals mainly with DC quantities. The computation is instantaneous but causes a time delay in filtering the DC quantities [15, 35, 44, 53, 55, 60, 65, 70, 72, 75, 82–84, 96–98, 112–119].

(viii) *Instantaneous symmetrical component theory*: In instantaneous symmetrical components method, a symmetrical voltage and current are transformed by symmetrical components to obtain positive sequence, negative sequence and zero sequence components of three phase variables. The instantaneous symmetrical component theory has advantages such as: it is simple in formulation, computationally less intensive for reference currents generation thus ensuring fast dynamic response and avoids interpretation of various definitions of instantaneous reactive powers and complex transformations. Numerous studies focused on symmetrical components theory were used for extraction the reference signal in [14, 35–39, 46, 48, 63, 68, 71, 98, 120, 121].

(ix) *Unity power factor theory*: This is another technique, except the fact that it forces the instantaneous current signal to track the voltage-reference waveform. This implies that the power factor would be fixed to unity and the system would only be suitable for the combined system of VAr and current harmonic compensation [58, 85, 98, 105].

(x) *Neural network (NN)-based theory*: NN-based algorithms are used to extract required information after processing of signals by learning or training and activation function. Arya and Singh [62], proposed an algorithm based on load conductance estimation using NN is implemented on a three phase DSTATCOM. Its structure is

reflected as Kohonen learning or Kohonen feature maps. It is used for extraction of fundamental component of load currents in terms of conductance and susceptance. Arya *et al.*, [122] proposed a NN based Anti-Hebbian control algorithm for PQ improvement under linear/non-linear type consumer loads which is used for extraction of fundamental active and reactive power components of load currents in terms of weighted signals. Reference [123] used a NN based adjustable step least mean square (LMS) for signal extraction. It uses autocorrelation time mean estimate error signal for updating the step size in place of simple error signal.

(xi) *Back propagation (BP) based theory*: BP algorithm includes three steps namely, the feed-forward of the input signal training, calculation and BP of the error signals, and upgrading of training weights. Continuity, differentiability, and non-decreasing monotony are the main characteristics of this algorithm. It is based on a mathematical equation and does not need special features of function in the learning process. It also has smooth variation on weight correction because of batch updating features on weights. In the training process, it is slow because of more number of learning steps, but after the training of weights, this algorithm generates very fast trained output response [124].

(xii) *Learning vector quantisation (LVQ)-based theory*: It is a standard statistical clustering technique which is also known as special case of competitive network. The desired values are extracted through training of weighed values of load currents using the gradient descent method. In the training process, the desired signals are at the position of the learning stage. After training, LVQ network classifies the supply current vector by assigning it to the same class as the output stage. It has its weighted vector closest to the input vector. In the LVQ network, each unit has a known value or elements and used supervised learning which differed from the Kohonen self-organising map [125].

(xiii) *Adaptive-based theory*: It is a closed loop controller that can adjust system behaviour in terms of response to disturbances. An area of adaptive control provides an automatic adjustment of the controller gains and parameters in real time, to achieve a desired level of performance. Characteristics of these control algorithms are the ability to extract required information from real online data to tune the controller, and also used for grid synchronisation. Based on this control theory, many control algorithms are also reported in available literature such as adaptive nature for synchronous extraction [103], adaptive theory-based improved linear sinusoidal tracer [13], adaptive control strategy based on artificial immune system [115] and leaky LMS adaptive filter [126].

(xiv) *Composite observer-based theory*: Composite observer is used to extract individual harmonics from repetitive signals. The settling period and the bandwidth of the observer depend on how far the observer poles have been placed from the origin of the S -plane or the Z -plane. The errors in the magnitude and phase of the extracted components, because of the deviation of the signal from the central frequency of the observer, are made very small by providing an integrated phase-locking arrangement. Further improvement in the accuracy, particularly in the extracted higher harmonics, is because of the introduction of multi-rate sampling. Advantages of this algorithm are that it is less sensitive with supply frequency variation, low distortion in the extracted signal without leakage of harmonics and so on [127, 128].

(3) *Other algorithms*: There are numerous optimisation and estimation techniques such as adaptive linear neuron (ADALINE) [97], LMS-based ADALINE [129], differential evolution [130], time-varying Fourier coefficient series [64], Fortescue decomposition with recursive DFT [131], peak detection [132], based algorithms used to extract the reference signal.

4.2 Current control techniques

Generation of suitable switching signal is the most significant part of DSTATCOM's control algorithm and has a high influence on the compensation performance [26]. PWM is the most reliable way of reconstructing a desired output voltage waveform. The frequency

of the switching should be significantly higher than that of the desired signal for a reliable signal representation [7]. PWM methods are often categorised as open loop (feed-forward) and closed loop (feed-back) methods. The open loop method is subdivided into SPWM and space vector PWM (SVM). The closed loop method are classified into hysteresis current control and linear current control involving ramp comparison, state feedback, synchronous vector, predictive, deadbeat, sliding mode, linear quadratic regulator, pole shift controllers. Apart from these methods the selective harmonic elimination technique also used for generation proper switching signal. Fig. 21 illustrates the classification of current control methods used in DSTATCOM.

4.2.1 Open loop PWM methods: SPWM: In SPWM, a sinusoidal reference signal is compared with a triangular carrier waveform to generate switching signals. The multi-carrier SPWM control methods were used to increase the performance of inverter, especially in multilevel inverter based DSTATCOMs. The multi-carrier SPWM can be categorised according to vertical or horizontal arrangements of carrier signal. The vertical multi-carrier SPWM techniques are identified as level shifted (LS-PWM), which includes phase disposition (PD-PWM), phase opposition disposition (POD-PWM) and alternative phase opposition disposition, while horizontal multi-carrier SPWM is defined as phase shifted (PS) control technique [14–17, 59–61, 70, 75, 82–84, 101, 111, 124, 133–136].

Space vector modulation (SVM): The goal of the SVM is to find the proper switching combinations and their duty ratios according to certain modulation scheme. SVM uses the control variable given by the control system and identifies each switching vector as a point in complex space of (α, β) . SVM operates in a complex plane divided in the six sectors separated by a combination of conducting or non-conducting switches in the power circuit. Although with the good reliability and strong anti-jamming of digital control technique, SVM is of low speed of response caused by the inherent calculation delay [137]. The main feature of the SVM switching strategy is that it enables to control the DC voltage and can balancing voltages of the DC capacitors in multilevel inverter, with no requirement of additional controls or auxiliary devices [93]. With SVM method, it is also possible to reduce THD and to solve the voltage unbalance problem [64, 65].

4.2.2 Closed loop PWM methods: Hysteresis controller: Hysteresis control is a widely used current control technique in the DSTATCOM applications because of its ease of implementation, fast dynamic response and inherent peak current-limiting capability [63]. The basic principle of current hysteresis control technique is that the switching signals are derived from the comparison of the current error signal with a fixed width hysteresis band. To bring the switching frequency to acceptable level for practical devices, hysteresis logic with suitable width (h) is required. The various switching schemes of hysteresis controller to achieve the desired switching frequency are two-level switching [30, 65], basic three-level switching [30, 65] and forced switching [30].

4.2.3 Second and higher order systems: Ramp comparison controller: The ramp comparison current controller also called as the stationary controller, uses three proportional-integrator controllers to provide a high DC gain, which eliminates steady-state errors and provides a controlled of the high-frequency response. In this scheme, comparison with the triangular carrier signal generates the control signals (switching functions) [6, 69, 113].

Predictive and deadbeat controllers: This technique predicts the current error vector on the basis of the present error and the AC side parameters at the beginning of each sampling period. The voltage vector to be generated by PWM during the next sampling period is determined to minimise the forecast error [6].

(i) **Constant switching frequency predictive algorithm:** In this case, the predictive algorithm calculates the voltage vector commands once every sample period. This will force the current vector

according to its command. The inverter voltage and EMF voltage of the load is assumed to be constant over the sample period. The calculated voltage vector is then implemented in the PWM modulator algorithm, for example, space vector. Note that, while the current ripple is variable, the inverter switching frequency is fixed. The disadvantage of this algorithm is that it does not guarantee the inverter peak current limit [113, 138–140].

(ii) **Deadbeat controllers:** When the choice of the voltage vector is made to null the error at the end of the sample period, the predictive controller is often called a deadbeat controller. Among the additional information given to the controller, non-available state variables can be included. Their determination can require the use of observers or other control blocks, which often may be shared with the control of the entire scheme [131, 138–141].

(iii) **Linear quadratic regulator (LQR):** The basic principle of LQR involves choosing the positive definite state and control input matrices, Q and R that provide satisfactory closed-loop performance. The closed-loop eigenvalues are related to these weighting matrices. The LQR control not only ensures the stability of a closed loop system, but it is also a controller with robustness features, because of the wide gain and phase margins. Theoretically, it can provide a gain margin between -6 and $+\infty$ dB and a phase margin between -60° and $+60^\circ$. Besides, it provides a low sensibility of the complete system. Another important feature of the LQR is that it can tolerate the input non-linearities [12, 48, 68, 142, 143].

(iv) **Sliding mode (SM) controller:** SM can be used to achieve robust system performance against parameter variations and load disturbances. SM control scheme performs a high speed switching control law to drive the state trajectory of the plant onto a specified surface in the state space, and to keep the state trajectory on this surface for all subsequent time. When sliding on the sliding surface, the structure of the system is changed discontinuously according to the instantaneous values of the system states evaluated along the trajectory. Owing to the discontinuous change of the structure of the system, SM control system is insensitive to the parameter changes of the plant and the external disturbances. With the inherent robustness and switching characteristics of SM control, it is especially suitable in the applications of closed-loop regulation of DSTATCOM [61, 144, 145].

(v) **Pole shift controller:** This is a discrete-time control technique in which the open-loop system poles are radially shifted towards the more stable locations to form the closed-loop poles. The pole-shift control algorithm utilises the on-line updated auto-regressive moving average model parameters to determine the new closed-loop poles of the system that are always inside the unit circle in the z -plane. It achieves regulation of the system to a constant set-point in the shortest interval of time [7, 52, 146].

3) **Selective harmonic elimination PWM:** SHE-PWM is based on fundamental frequency switching method and realised to eliminate the defined harmonic orders. This method defines the switching angles of harmonic orders to eliminate and obtain the Fourier series expansion of output voltage. Basically, in SHE-PWM, the harmonic components of the predefined switched waveform with the unknown switching angles are bring to zero for those undesired harmonics, while the fundamental component is kept to the desired reference amplitude. SHE-PWM is a very attractive option for multilevel inverter applications, because the equipment requires operating at a very low switching frequency to decrease the power switches losses [21–23, 56, 66, 69, 147].

5 Classification of DSTATCOMs based on the compensated variable

The main aim of a DSTATCOM is to compensate different PQ problems (voltage quality problems such as sags, swells, flicker, unbalance, harmonics and current quality problems such as harmonics, reactive current, unbalance and neutral current) at PCC. DSTATCOM includes two modes of operation: Single mode and

Table 2 Classification of DSTATCOMs according to compensated variables

Compensated variables	Inverter topology	Current control method	Modulation strategy	Reference
Single mode reactive power	3-level NPC-MLI	time-varying Fourier	SV-PWM	[64]
	2-level PWM VSI	synchronous reference frame	hysteresis-based PWM	[96]
	2-level PWM VSI	synchronous reference frame	SPWM	[82]
	5-level DC-MLI	ins. symmetrical component	LQR	[68]
	3-level NPC-MLI	ins. symmetrical component	hysteresis-based PWM	[63]
	2-level PWM VSI	adaptive based on AIS	SPWM	[115]
	5-level CHB-MLI	sliding mode	hysteresis-based PWM	[74]
	2-level PWM VSI	sliding mode	carrier PWM	[33]
	2-level PWM VSI	$p-q$ theory	dead-beat	[148]
	voltage sag	2-level PWM VSI	inst. symmetrical component	SPWM
84-pulses VSI		synchronous reference frame	—	[79]
2-level PWM VSI		synchronous reference frame	—	[118]
voltage flicker	2-level PWM VSI	synchronous reference frame	SPWM	[117, 134]
voltage unbalance current harmonics	3-HB VSI	$p-q$ theory	pole-shift technique	[52]
	2-level PWM VSI	Fortescue with RDFT	dead-beat	[131]
voltage sag and flicker	3-HB VSI	Kalman filter	hysteresis-based PWM	[51]
voltage and frequency	2-level PWM VSI	synchronous reference frame	carrier PWM	[149]
reactive power and voltage control	11-level CHB-MLI	synchronous reference frame	PS-PWM	[150]
	—	synchronous reference frame	—	[151]
	2-level PWM VSI	synchronous reference frame	SPWM	[152]
	2-level PWM VSI	synchronous reference frame	SPWM	[83]
	5-level CHB-MLI	synchronous reference frame	SPWM	[75]
	2-level PWM VSI	synchronous reference frame	SV-PWM	[119]
	2-level PWM VSI	synchronous reference frame	hysteresis-based PWM	[112]
reactive power and unbalance load	2-level PWM VSI	ADALINE based	hysteresis-based PWM	[97]
	5-level CHB-MLI	synchronous reference frame	LS-PWM, PS-PWM	[15]
reactive power and current harmonics	2-level PWM VSI	synchronous reference frame	predictive	[113]
	2-level PWM CSI	fourier transform	SHE	[21]
	2-level PWM VSI	synchronous reference frame	SHE	[56]
voltage and voltage harmonic	CHB-MLI	synchronous reference frame	—	[132]
	single phase VSI	sliding mode	hysteresis-based PWM	[30]
voltage sag and swell with phase angle control	2-level PWM VSI	two-loop feedback control	dead-beat	[141]
voltage support and balance with angles control, balance the active and reactive power current harmonic and current unbalances	2-level PWM VSI	$p-q$ theory	SPWM	[153]
	2C-VSI	inst. symmetrical component	hysteresis-based PWM	[35]
	3HB VSI	inst. symmetrical component	hysteresis-based PWM	[45]
	3-level NPC	ins. symmetrical component	hysteresis-based PWM	[38]
	4 L VSI	ins. symmetrical component	hysteresis-based PWM	[41]
	3HB VSI	ins. symmetrical components	LQR	[48]
	2-level PWM VSI	synchronous reference frame	—	[116]
	2C-VSI	inst. symmetrical component	hysteresis-based PWM	[37]

Continued

Table 2 Continued

Compensated variables	Inverter topology	Current control method	Modulation strategy	Reference	
voltage regulation and unbalance	2-level PWM VSI	wavelet transform	SPWM	[84]	
	2-level PWM VSI	synchronous reference frame	SPWM	[154]	
voltage regulation, current unbalance and neutral current	3HB	$p-q$ theory	hysteresis-based PWM	[47]	
voltage sag and unbalance	7-level CHB-MLI	synchronous reference frame	—	[72]	
	2-level PWM VSI	synchronous reference frame	hysteresis-based PWM	[114]	
voltage sag, swell and unbalance	single phase VSI	phase space	carrier PWM	[31]	
current harmonics, unbalance and neutral current	$p-q$, crosse vector, vectorial, global, $p-q-r$, unity power factor, synchronous reference frame, instantaneous symmetrical components			[98]	
current harmonics, unbalance and neutral current	3HB VSI	ins. symmetrical component	hysteresis-based PWM	[46]	
	2-level PWM VSI	synchronous reference frame	SPWM	[60]	
	2-level PWM VSI	NN	—	[62]	
	2-level PWM VSI	single phase $p-q$ theory	—	[155]	
current harmonics and unbalances	5-level FC-MLI	ins. symmetrical components	hysteresis-based PWM	[71]	
	3HB VSI	ins. symmetrical component	hysteresis-based PWM	[120]	
	2-level PWM VSI	unity power factor	hysteresis-based PWM	[85]	
	2-level PWM VSI	composite observer-based	SPWM	[127]	
	2-level PWM VSI	LMS based ADALINE	hysteresis-based PWM	[129]	
	3HB	$p-q$ theory	hysteresis-based PWM	[49]	
	reactive power, current harmonic, current unbalances and voltage control	2-level PWM VSI	$p-q$ theory	hysteresis-based PWM	[100]
		2-level PWM VSI	synchronous reference frame	—	[53]
reactive power, current harmonics and neutral current	5-level CHB-MLI	$p-q$ theory	PS-PWM	[59]	
	<i>Dual mode</i>				
voltage sag or current harmonics	3-level FC-MLI	synchronous reference frame	PS-PWM	[70]	
current harmonics, unbalance and neutral current or voltage regulation, current harmonics, unbalance	4 L VSI	inst. symmetrical component	—	[40]	
	2-level PWM VSI	adaptive theory	—	[13]	
voltage unbalance or current harmonics, unbalances and neutral current	4 L VSI	$p-q$ theory	hysteresis-based PWM	[45]	
	2-level PWM VSI	admittance based	—	[57]	
reactive power and current harmonics or voltage regulation	2-level PWM VSI	$p-q$ theory	SPWM	[101]	
load balancing and current harmonics or voltage regulation	2-level PWM VSI	NN based adjustable step LMS	—	[123]	
	2-level PWM VSI	NN based anti Hebbian	—	[122]	
	2-level PWM VSI	leaky LMS adaptive filter	—	[126]	
	2-level PWM VSI	back propagation	SPWM	[124]	
	2-level PWM VSI	$p-q$ theory	—	[102]	
	4 L VSI	synchronous reference frame	SPWM	[44]	
reactive power, current harmonics, neutral current and load balance or voltage regulation, current harmonics, neutral current and load balance	2 leg VSI	synchronous reference frame	SPWM	[55]	
	2-level PWM VSI	unity power factor	SPWM	[58]	
	2-level PWM VSI	syn. detection algorithm	—	[153]	
reactive power, current harmonics, and load balance or voltage regulation, current harmonics and load balance	2-level PWM VSI	adaptive filter	—	[103]	
	2-level PWM VSI	peak detection	—	[132]	

NPC-MLI (Natural point clamped multilevel inverter), DC-MLI (Diode clamped multilevel inverter), FC-MLI (Flying capacitor multilevel inverter), CHB-MLI (Cascaded H-bridge multilevel inverter).

dual mode. In single mode, the problems related with current or voltage can be compensated. In dual-mode, according to importance of problems related with current or voltage, DSTATCOM can enter in either current or voltage control mode. The classification of DSTATCOMs according to compensated variables is presented in Table 2.

6 Latest trends and practical considerations

Through qualitative improvement and rapid commercialisation of high power switching devices and high performance digital signal processors, DSTATCOMs has been developed with high performance, more functionalities and low costs. Design and development of high capacity DSTATCOMs based on multilevel inverter topologies are the new and interesting research area in PQ conditioners field. Moreover, to mitigate the PQ disturbances, the control strategies applied to DSTATCOMs will play significant role. So, optimising the control strategies and executing multifunctional control are the main research trend.

The application of renewable energy systems (RESs) as a source of electrical energy in the DG systems is gaining more attention with the advances in power electronics technology. The key component in the RESs based DG systems is grid connected inverter that interfaces the RESs with the utility grid. The application of DSTATCOMs as interfaces the RESs with the utility grid not only perform the high quality power from RESs, but also provide increased functionality through improved PQ, voltage and reactive power support and increase the capability of the auxiliary service for utility grid. The development of new control strategies and execution of multifunctional compensation capabilities in RESs are the main research trends related to both active power flow control and mitigation of various PQ disturbances using DG-DSTATCOM.

There are also some papers presenting the performance comparison of commonly used topologies and controller. In [156], three commonly types of inverters were designed for a 6.6 kV-12MVA DSTATCOM and the operational losses and costs were compared. In the comparison of operational losses, the DC-DSTATCOM had the smallest loss and the CHB-DSTATCOM had the highest loss. Even though the FC-DSTATCOM loss is almost 7% higher than the DC-DSTATCOM, the FC-DSTATCOM is more attractive, because IGBTs of FC-DSTATCOM have homogeneous loss distribution. In the comparison of costs, costs of inverter units, inverter cabinets and capacitor banks were estimated. As a result, the cost of DC-DSTATCOM was the highest, because clamping diodes of DC-DSTATCOM are expensive and it needs complicated bus bars. The cost of FC-DSTATCOM was nearly equal to the cost of CHB-DSTATCOM. The losses and costs are the most important factors for an inverter design. From this comparison using present day available components, it is clear that the FC-DSTATCOM is the most attractive topology for a 6.6 kV DSTATCOM.

By increasing interest on PQ from both end users and power suppliers, the DSTATCOM applications are becoming

commercially available with the advanced power electronics and smart control methods. Table 3 presents the installed DSTATCOMs at different capacity in various commercial applications.

In practical applications, the selection of the DSTATCOM structure is an important task for scientists and engineers. The main design considerations for proper selection of inverter topology are

- (i) Output voltage level.
- (ii) Power rating.
- (iii) Current/voltage distortion level.
- (iv) dv/dt stresses level.
- (v) Common-mode voltage level.
- (vi) Manufacturing cost level.

7 Conclusions and future scope

This paper presents an exhaustive review and discussions on the DSTATCOMs to improve the PQ at utility grid and industrial facilities. Different aspects of DSTATCOMs and new developments in this field of research have been discussed in detail to highlight their advantages and disadvantages. The review and classification of research articles published conclude that DSTATCOMs can be beneficial to mitigate both current and voltage related PQ disturbances.

Development of new control strategies and execution of multifunctional compensation capability are the main research trends to perform mitigation of various PQ disturbances using DSTATCOMs. DSTATCOMs are essentially candidate for the future utility grid and industrial facilities to perform high quality, reliable and efficient of electricity supply. To achieve this goal, various topologies and structures should be employed to increase the capacity of installed DSTATCOMs. The future research fields on DSTATCOM technology can be summarised by the following goals:

- (i) Novel control algorithms should be developed to increase the capability of DSTATCOMs for simultaneous mitigation of multiple PQ problems.
- (ii) There is a lack of research studies about the simultaneous compensation of flicker and harmonics on DSTATCOMs.
- (iii) There are not enough research studies on DSTATCOMs to extract and eliminate the interharmonic components.
- (iv) A detailed analysis of various phase control techniques for DSTATCOMs should be realised.
- (v) There is not any research study focusing specifically on the compensation of asymmetrical unbalance in the voltage (unbalance in both the phase and magnitude of the voltage).
- (vi) New switching methods should be introduced to reduce the harmonic contents of the inverter current.
- (vii) Investigation of the use of current source multilevel inverters in the DSTATCOM technology should be considered.
- (viii) LCL or LLCL filters are recently used in DSTATCOM applications to provide a superior harmonic spectrum for the injected current. However, to overcome resonance risk in these types of filters and to maintain the inverter output voltage to its nominal voltage, novel control algorithms should be developed.

The comprehensive review of DSTATCOM will help researchers, users and suppliers of electrical power to gain an overview for further research and studies on this subject.

8 Acknowledgments

The authors gratefully acknowledge the Electrical, Electronics and Informatics Research Group of Scientific and Technological Research Council of Turkey (TUBITAK) for the research project (project number: EEEAG – 114E015).

Table 3 Capacities and application areas of installed DSTATCOMs

Reference	Capacity	Application
[157]	±75 kVAr	distribution substation
[158]	±250 kVAr	distribution substation
[154]	300 kVAr	iron and steel corporation
[159]	500 kVAr	steel plant
[22]	–500/750 kVAr	lignite mining
[21]	±750 kVAr	coal mining excavators
[160]	2.5 MVar	steel plant
[161]	3 MVar	wind turbines
[162]	5 MVar	iron & metals corporation
[22]	–5.1/0 MVar	coal conveyor belt drives
[163]	8 MVar	wind farm
[164]	±60 MVar	steel plant
[165]	±80 MVar	steel plant

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